FEDERAL TRADE COMMISSION

I N D E X (PUBLIC RECORD)

UNITED STATES OF AMERICA

FEDERAL TRADE COMMISSION

In the Matter of:)

Rambus, Inc.) Docket No. 9302

----------)

Monday, June 2, 2003

1:00 p.m.

TRIAL VOLUME 20

PART 1

PUBLIC RECORD

BEFORE THE HONORABLE STEPHEN J. McGUIRE

Chief Administrative Law Judge

Federal Trade Commission

600 Pennsylvania Avenue, N.W.

Washington, D.C.

Reported by: Josett F. Hall, RMR-CRR

For The Record, Inc.
Waldorf, Maryland
(301) 870-8025

APPEARANCES:

ON BEHALF OF THE FEDERAL TRADE COMMISSION:

M. SEAN ROYALL, Attorney
GEOFFREY OLIVER, Attorney
JOHN C. WEBER, Attorney
MICHAEL FRANCHAK, Attorney
ROBERT DAVIS, Attorney
Federal Trade Commission
601 New Jersey Avenue, N.W.
Washington, D.C. 20580-0000
(202) 326-3663

ON BEHALF OF THE RESPONDENT:

GREGORY P. STONE, Attorney
STEVEN M. PERRY, Attorney
PETER A. DETRE, Attorney
SEAN GATES, Attorney
ANDREA WEISS JEFFRIES, Attorney
Munger, Tolles & Olson LLP
355 South Grand Avenue, 35th Floor
Los Angeles, California 90071-1560
(213) 683-9255

APPEARANCES:

ON BEHALF OF THE RESPONDENT:

A. DOUGLAS MELAMED, Attorney
Wilmer, Cutler & Pickering
2445 M Street, N.W.
Washington, D.C. 20037-1420
(202) 663-6090

P R O C E E D I N G S

- - - - -

JUDGE McGUIRE: This hearing is now in order.

Counsel, I want to take up a couple housekeeping items before we start today.

First of all, regarding the opposition to the proposed testimony of Dr. Oh, I just received the response to that opposition about two hours ago. I am currently involved in trying to draw up an order on that and I anticipate being able to have that order issued on Tuesday morning, so we'll anticipate having that issued at that time.

The other item I want to take up is I've been informed that I'm going to have to attend a conference, I'm obligated to attend a conference on Friday, June 13, and that is to run from 9:00 a.m. through 12:00 noon, so I will be happy -- we can I guess convene the hearing at any time on that date after 12:00, or if it's going to cause too much problem, we can go to trial as well on I guess this coming Friday. I know we're otherwise off on our schedule, but if that would help overcome some of that, or we could start on that Friday at 12:30 and go late if we have to.

So I'm just going to advise everyone of that

change in schedule.

Mr. Oliver, go ahead.

MR. OLIVER: Just on scheduling issues, I will have to check our calendar to see how that affects us and what we might be able to do. I did want to remind you that we were planning to have next Tuesday and Wednesday off, and as a result of that we were planning to be in schedule next Friday.

JUDGE McGUIRE: I'll tell you what this is. This is not of my own choosing. As a supervisor of an office here in this FTC agency I'm required to attend a three-hour training session for my employees. I understand that is being offered on other dates. I will see if I can change to either what would be Tuesday, the 10th --

MR. STONE: 10th and 11th we claim to be dark.

JUDGE McGUIRE: Let me see if I can't get that changed. Otherwise, that was the only time they had. And perhaps I can send an e-mail and say I want out of this, I want to opt out, and we'll see what happens, but I'll see if I can get that changed to try and keep the hearing on track.

MR. STONE: Okay.

JUDGE McGUIRE: Anything else, Mr. Oliver?

MR. OLIVER: No. Other than that, we can check

with our schedule of witnesses to see.

JUDGE McGUIRE: I'll have an answer on that in the morning.

MR. STONE: Okay. And so your plan is at the moment at least we're scheduled to be dark this Friday.

JUDGE McGUIRE: That was the plan, but I'm open as well. I want to keep this thing on track, and I know we've had a few off days here and -- but I thought that was our understanding, but I'm free to do whatever the parties can do, and I know that puts the onus on the FTC in that regard.

MR. STONE: I think they might have been planning to go forward on Friday.

JUDGE McGUIRE: Okay. Then let's go forward on Friday.

MR. OLIVER: I should have been clear on our schedule.

JUDGE McGUIRE: I didn't assume that. I thought we wouldn't be going on Friday.

So we will be going this coming Friday, the 6th.

MR. OLIVER: If that's okay with you. We thought that by having next Tuesday and Wednesday off --

JUDGE McGUIRE: No. I didn't realize that, so that's fine. So that would make it imperative then to try to change the schedule if I could for the following Friday if we're going to be off on Tuesday and Wednesday.

MR. STONE: If you can, but if we lose a half a day --

JUDGE McGUIRE: If we do, we do. I'll do what I can do about it, but I'm not in charge, so we'll see.

Mr. Stone, anything you want to add?

MR. STONE: I just want to introduce one of my partners. Andrea Weiss Jeffries is going to be here. Mr. Detre will be back. His wife is going to be due any day now, so she's come to help us.

Then I want to move in RX-2302, which was the press release that I used on Friday.

JUDGE McGUIRE: Mr. Oliver, any objection?

MR. OLIVER: No objection, Your Honor.

JUDGE McGUIRE: All right. So entered at this time.

(RX Exhibit Number 2302 was admitted into evidence.)

MR. STONE: Okay, Your Honor.

JUDGE McGUIRE: Okay. Very good.

At this time then the complaint counsel may call its next witness.

MR. DAVIS: Thank you, Your Honor.

Complaint counsel calls Steve Polzin.

JUDGE McGUIRE: Sir, would you please come toward the bench and the court reporter will swear you in.

- - - - -

Whereupon --

STEVE POLZIN

a witness, called for examination, having been first duly sworn, was examined and testified as follows:

JUDGE McGUIRE: You may proceed, Mr. Davis.

MR. DAVIS: Thank you, Your Honor.

DIRECT EXAMINATION

BY MR. DAVIS:

Q. Please state your name for the record.

A. Steve Polzin.

Q. And where are you currently employed?

A. AMD, Advanced Micro Devices.

Q. What's your position at AMD?

A. They call me the chief platform architect.

Q. And what are your responsibilities in that position?

A. My responsibilities are to ensure that there

are competitive components that surround the microprocessors that AMD designs and sells. That includes chipsets, motherboards, DRAM, voltage controllers, clock chips, everything that surrounds the microprocessor to make competitive computers for our customers.

Q. How long have you been the chief platform architect at AMD?

A. I think they gave me that title in 2001.

Q. And what was your position prior to that?

A. Before that, they referred to me as the Athlon system architect where I was focusing on Athlon, our previous-generation microprocessor.

Q. What were your responsibilities in that position?

A. Very similar to what I described, but at that point I was focused on just one product.

Q. Did you have a position prior to that at AMD?

A. Prior to that, I was a design manager that managed the chipset group for -- that was designing a chipset for K7, for Athlon, the Northbridge portion of that chipset.

Q. What were your responsibilities in that position?

A. Managing the team that did the design and

implementation of the Northbridge for K7, so I manage the team, drive the schedule, drive the project.

Q. Were there any code names for that particular chipset?

A. Yeah. The K7 or Athlon Northbridge chipset was referred to internally as Irongate or IG.

Q. Did you have a position prior to that at AMD?

A. Before that, I managed pretty much the same team working on a K6 Northbridge chipset.

Q. And how long have you been at AMD?

A. June 1996 is when I joined.

Q. And prior to that where were you?

A. I was at Apple Computer.

Q. And what did you do there?

A. At Apple Computer I was the -- they called me the hardware lead or the system architect for power Macintosh computers.

Q. And what did you do in that position?

A. Pretty much similar to what I described as the system architect at AMD but more detailed. I managed multiple designers working on chipsets in the memory controller, the I/O controller. Details of the motherboard design I worked on, system-level design aspects, file cards in mechanicals, that sort of thing.

Q. Did you have any responsibilities at Apple with respect to DRAM?

A. Yes. My team was the team that designed the memory controller chip.

Q. Did Apple use SDRAM while you were at Apple?

A. Not to my knowledge. Not in the product I was working on.

Q. Were you aware of whether Apple was considering using SDRAM while you were employed there?

A. We had considered that. Our procurement manager, the folks that are in charge of buying components for our -- for Apple products, kept us aware of industry developments, and synchronous DRAM was on the horizon. We chose not to implement it for the machine that we introduced in 1995.

Q. And why did you choose not to implement it?

A. I'm sorry? Why?

Q. Why did you choose not to implement it?

A. The main factor was it was too new. It wasn't in the price point that was established to be a commodity. We didn't want to be disadvantaged when customers bought a Macintosh that they would have to buy more expensive memory than buying a PC, for example.

The commodity DRAM at the time was not

synchronous DRAM. The commodity DRAM was fast page mode or EDO. I forget exactly which one was the commodity at the time, but it wasn't synchronous. Synchronous was too new.

Q. You've used the term "commodity." How have you been using that term?

A. "Commodity" means widely available at a low cost and it generally means multiple manufacturers make the same part and they compete on cost.

Q. And how long were you at Apple?

A. 1992 to 1996, almost five years.

Q. And were you employed prior to being at Apple?

A. I was employed at the Digital Equipment Corporation in Massachusetts.

Q. And what did you do, briefly, at Digital?

A. Lots of things. I started out in 1983 as a young, green kid right out of school doing low-level chip design in a large VAX computer and held various positions designing system-level components up to my final position, which was system architect for a multiprocessor Alpha-based server system.

Q. Okay. And were you employed prior to being at Digital?

A. I was in school.

Q. Where were you in school?

A. I have a BSEE from the University of Connecticut.

Q. That's a bachelor of science in electrical engineering?

A. Yes, sir.

Q. Since you've been at AMD, how many different CPU generations have you worked on?

A. K6, K7, K8, and we're working on K9.

Q. Does AMD sell chipsets for those CPUs?

A. AMD sold chipsets for K7 and K8. We haven't sold K9 yet, so we haven't sold the chipsets for it yet.

Q. AMD didn't sell chipsets for the K6?

A. I don't think it did. I'm not quite certain on whether we actually -- we worked on a design for one, but I believe we chose not to take it to market.

Q. And why was AMD developing chipsets to work with the K6?

A. The K6 microprocessor was pin compatible with an existing Intel microprocessor, the Pentium, and therefore we were able to sell our microprocessors to folks that could get a motherboard that was compatible with a Pentium. There was an existing infrastructure of motherboards for Pentium that K6 fit into very well, seamlessly.

We, AMD, were fearful that Intel was moving away from that Pentium infrastructure and they were going to a Pentium II infrastructure and they were going to leave that infrastructure behind and we wouldn't have anywhere to plug in our microprocessor, so we thought we needed to continue that motherboard infrastructure with our own chipset.

Q. Did AMD sell chipsets for the K7?

A. Yes.

Q. And what was your understanding of the business purpose for AMD to sell chipsets for the K7?

A. With K7, we developed a unique interface to our microprocessor, the so-called front-side bus. We did not copy Intel or follow Intel at that time. We licensed a design from Digital Equipment Corporation that was used on the Alpha microprocessor.

We called that the S2K, which stood for Socket 2000, just a geeky term, but that was a unique thing to AMD and we needed to design a chipset that interfaced to it to get our motherboard partners developing motherboards that would be compatible with K7 and also provide the design as a design example for our chipset partners so that they could design chipsets that supported K7.

Q. Now, with regard to the K8, does AMD plan on

selling chipsets for the K8?

A. Yes, and we are currently. We have introduced that part. However, K8 has a radically different system architecture, so while we do sell components that can be referred to as chipsets, they don't include the memory controller anymore. We've moved the memory controller onto the K8 microprocessor device.

Q. Do you have an understanding of why AMD chose to move that onto the K8 microprocessor?

A. The reason we moved the memory controller onto the microprocessor was to gain significantly more performance out of the microprocessor by moving memory logically closer in terms of latency to the microprocessor.

Q. Did you have any role in the decision to include that on the K8?

A. Yes.

Q. And what did you understand to be the benefits to AMD for including the memory controller on the microprocessor design?

A. Performance. We were able to deliver significantly better performance delivered to the customer by having the DRAM very close.

Q. That's what I'm wondering. What do you mean by

"performance" in this case?

A. Oh, okay. The way microprocessors work is they're executing a program and they need to access data that is not contained locally in the microprocessor. It needs to go out to main memory to get that data.

In the old, traditional way, that request would have to go from the microprocessor across the motherboard to the chipset. The chipset would have to figure out what to do, Northbridge chipset. It would then send that request to the memory. It would wait. The memory would return the data. The data again would have to go through that Northbridge chipset again across the motherboard to the microprocessor. That's a long time.

If the memory controller is integrated with the processor, that time can be cut down significantly, allowing programs to execute faster.

Q. Do you have an understanding of whether the K8 is designed to work with any particular kind of DRAM?

A. Yes. It's designed to work with DDR DRAM.

Q. I understand DDR has a number of different speeds. Is it designed to work with any particular speed of DDR DRAM?

A. We designed it to run with DDR 200, 266, 333

and 400.

Q. Are you aware of whether AMD has attempted to develop products for use with RDRAM?

A. Yes.

Q. And what was AMD attempting to make work with RDRAM?

A. We were planning to have the follow-on chipset for K7 support RDRAM.

Q. And what was your role in this project?

A. I was again the design manager of the team.

Q. Was there a code name for this project?

A. Yes. The code name for that project was IGR4.

Q. And what did that stand for?

A. So IG is Irongate from the original chipset, R was Rambus, and 4 was 4XAGP, which is the graphics support that we also put on that second-generation chip.

Q. When did that activity take place?

A. I believe we started up the design team working on it in earnest in the fall of 1998.

Q. And were you aware of how the decision was made at AMD to begin this project?

A. Yes.

Q. Did you have any role in this decision?

A. Yes.

Q. And why was RDRAM chosen?

A. We had -- we have an ongoing series of meetings with our DRAM partners as just normal course of business, and they were telling us in '97 and early '98 that it was very clear that Intel was going to go to Rambus pretty much across the board, they were going to make Rambus the standard in the industry, jam it down our throats. We sort of had no choice.

Q. Why was that important, why was Intel's adoption of Rambus important to AMD?

A. They drove the volume, and if the volume DRAM was Rambus, that would become the commodity part, and we had to remain competitive in terms of both performance and cost, and if the indications were most of the DRAMs to be built in the world were going to be Rambus DRAMs, we better be compatible with them.

Q. Do you know whether AMD was originally planning to use RDRAM with the K7 as the follow-on to PC133?

A. The -- there was a series of evaluations done to determine what the right memory should be for K7 to follow on to the original chipset. There was a discussion on whether it should be DDR or Rambus or whatever options were out there.

Q. Now, what was your impression of DDR at this point?

A. Well, DDR in I guess '97 or so was not in very good shape. A lot of the DRAM folks were very supportive of it and were pushing it and saying this is a great technology. The problem was that the technology was addressed at a component level. The DRAM manufacturers were specifying a component, a DRAM component.

There were no other chipset folks signed up that we knew of. No one had looked at the system-level aspects of implementing DDR. No one had laid out a DIMM, a DIMM module, for example. No one had figured out the placement for termination resistors, enabled clock chip vendors, power supply vendors, et cetera. There was a lot of work left to be done.

Additionally, the DDR DRAMs being offered by the DRAM companies differed slightly in between company to company. One company would have a slightly different spec than the other one. It wasn't a unified spec at that point.

Q. What was the importance of there being different specs between the different DDR manufacturers?

A. That would have been very bad to design a memory controller to work with different flavors of the same device. It was crucial that we design systems that could accept a DDR device from any manufacturer, again, to get to that commodity state where many manufacturers offer the same device at low cost.

If the devices were different in slightly different ways, it would cause incompatibilities or force the memory controller design A and B to implement all sorts of weird hacks and it would just be a mess. It was crucial that we had a common standard that would allow interoperability.

Q. I'd like to show you a document that's been marked for identification as CX-2153. I hope we have a copy of it there.

A. Yep.

MR. GATES: Do you have a copy for me?

MR. DAVIS: Yes. I'm sorry.

BY MR. DAVIS:

Q. Do you recognize this document?

A. Yes.

Q. And what is it?

A. It is an e-mail that I wrote in response to a note from Eric Hsu, who was an account representative in our infrastructure enablement group. I believe he

was responsible for the Samsung relationship at this point.

Q. Now, at the bottom of the e-mail -- at the bottom of the document is an e-mail from Eric Hsu to you.

What was your understanding of what he was telling you in this e-mail?

A. At this point in time Samsung was trying to have us adopt DDR for our K7 chipset, our follow-on K7 chipset, and they would come and present us information and I would ask, well, we need, you know, A, B, C, D, you know, a list of things we needed to help us make the decision one way or another, and Eric was saying that his contacts at Samsung were calling to make sure I had all the information I needed.

Q. What sort of information was Samsung offering you?

A. They were offering device specifications.

Q. Was that the information that you were interested in receiving?

A. No. There were two main points. We needed more of the system-level information. We needed the layout design guidelines, a DIMM specification, a DIMM layout, termination guidelines, power supply, clock chips. The whole system solution is what we were

really looking for.

In addition, we were looking for Samsung -- actually we were asking all of our memory partners to work through a common spec using JEDEC, given that they all had slightly different specs in various points.

Q. So if you look at the top e-mail, which is your e-mail to Eric Hsu, and item number 1 -- actually right before you say, "What we need information on and I still claim that we do not yet have is specifically, one, a JEDEC DDR spec that is vendor neutral."

What did you mean by that?

A. We needed a spec that was common so that our memory controller could be designed to one spec and be assured of working interoperably with devices from all manufacturers, all DRAM manufacturers.

Q. And below that you stated in the e-mail, "I stated to Samsung that it would be a huge effort on our part to resolve the numerous differences between vendors."

Now, what would be a -- why would it be a huge effort to resolve those differences?

A. What I meant there is it's a huge effort outside JEDEC. JEDEC was the natural forum and process for resolving the numerous differences. I was stating,

if AMD tried to do that on their own, it would be a huge effort on our part.

Q. And 2 of the e-mail under the information you wanted states, quote, "The Samsung person that I spoke to also agreed that the system-level stuff was not very well understood. I pointed out that the difficulties that Intel had getting PC100 DIMMs correct and we agreed this would be a big effort."

What did you mean by a system-level spec and design guide? I think you referenced those.

A. That's exactly what I meant.

Q. And what is a system-level spec with a design guide?

A. A design guide, a system-level planning budget, termination resistor placement, termination guidelines, voltage regulator specs, clock specs, et cetera.

Q. And why are these important to AMD in whether they're going to adopt DDR?

A. To get all of that, all those specifications, correct required a lot of work, and AMD at this point wasn't prepared to do all that work by ourselves. We were hoping that an industry consortium, you know, the -- everybody would work together to arrive at the right answer.

MR. DAVIS: I'd like to move CX-2153 into evidence.

MR. GATES: No objection, Your Honor.

JUDGE McGUIRE: Entered.

(CX Exhibit Number 2153 was admitted into evidence.)

BY MR. DAVIS:

Q. Could you describe the work that was done at AMD in order to allow the K7 to work with RDRAM.

A. That would be the design of the IGR4 Northbridge chipset, and the work that was done there was broken into two parts.

The first part was the actual design of the chipset itself. We started with the base Irongate design -- that was the IG -- and added a Rambus memory controller to it.

In parallel, part of the deal that was arrived at with Rambus was that Rambus was going to design the I/O cell. There's a complicated set of logic and analog circuitry called a rack that needs to be designed very, very carefully, that Rambus does that design in the semiconductor process of interest for the partner.

So Rambus did that design for us. We took that information and taped it out on a test chip and into

the semiconductor fabrication facility that we were going to use, which I believe was UMC at this point, and we built a package for it and built the part and got it back and tested it and qualified it, made sure that that design was solid for later inclusion in the main part.

Q. Do you know if AMD ended up implementing the Irongate Northbridge for DRAM?

A. We brought it to the point of pretty much completion of the design, but we decided late in the design not to tape it out but rather to put the project on the shelf for later, later production possibly.

Q. What do you mean, put it on the shelf?

A. We took the design database and added the libraries and the CAD tools and the system-level elements in a big data backup so that we could, when we chose to restart the project, we could just immediately take this whole design environment and restart it. And we put that all on an archival data storage.

Q. What was your understanding or what is your understanding of the reasons that AMD stopped development work on the Rambus Northbridge for the K7?

A. There were a couple of reasons. The main

reason was that we had earlier decided to start a parallel effort designing a DDR chipset and we decided that there was a lot of work to bring both of those to market and we needed some resources freed up from the IGR4 team to help out our microprocessor design effort at the time.

Q. I'd like to show you a document that's been marked for identification as CX-2158.

A. Okay.

Q. Do you recognize this document?

A. Yes.

Q. Did you write this document?

A. Yes.

Q. Why did you write CX-2158?

A. I was requested to give a quick history of our engagement with Rambus and DDR to Dirk Meyer.

Q. And who is Dirk Meyer?

A. Dirk Meyer at that point was vice president of microprocessor design in our group.

Q. Did you do anything to arrive at the information that was presented on CX-2158?

A. Yeah. I most likely went through my e-mail folders and probably through my notebooks to get the dates right, put it in chronological order.

Q. I'd like to take a look at this document if we

can.

The first bullet says, "Initial direction was DDR main memory for K7," and then it says, "Top-level DDR attributes were very attractive to K7."

What did you mean by that?

A. K7, when we designed it, we aimed for clear leadership performance in the marketplace, and a large part of microprocessor performance is memory bandwidth, and they designed -- one of the reasons that we designed our own front-side bus, we adopted the S2K, was that had offered much higher performance, much higher bandwidth capabilities, and the initial look out into the DRAM industry suggested that DDR DRAM had bandwidth numbers that matched what we were looking at for K7, so it seemed like a good match, just on a performance bandwidth perspective.

Q. Okay. Below that the note that there were discussions with Samsung, Micron and NEC it looks like May of 1997?

A. Yes.

Q. And it quickly became apparent, and there's a number of bullets below that.

First, it says "not one standard" and I think you've already talked about that?

A. Yes.

Q. There are a couple of sort of technical things, different I/O voltages, different protocols.

What were you referring to there?

A. Some manufacturers were attempting to start DDR using 3.3-volt I/O signaling and others were going to 2.5 volt. There was no commonality between a few of them.

The differing protocol, some manufacturers were proposing bidirectional strobes, others were proposing no strobes. It was just basic parts of the protocol just were not nailed down in common between all the manufacturers.

Q. You just mentioned the term "strobe." What do you mean by that?

A. A strobe is a signal that is used to qualify data transfers. When data is transferred between the DRAM and the memory controller.

Q. What do you mean, "qualify data transfers"?

A. Consider it a clock. It's a clock that goes along with the data to specify where a data bit starts and ends.

Q. Below that you say "no DIMM infrastructure planned" and then in parentheses you say "two DIMM standards."

What did you mean by a DIMM infrastructure?

A. Back to some of what I said earlier, no one had come up with a common DIMM. DIMM stands for dual in-line memory module and it's the circuit board that has the DRAM component soldered to it for eventual -- the DIMM gets plugged into the motherboard.

And there were -- there were no common DIMM standards. Everybody had a slightly different version of it, different pinouts, different form factors. Again, back to the commodity statement, it's crucial that we have a common standard for the DIMM definition so that anybody's DIMM plugs into the motherboard and works just fine.

Q. Now, below that you say, "No support components, power supply, clock chips and registers."

What were the importance of -- first of all, what's a clock chip and what's a register?

A. A clock chip is a chip, you know, an electronic circuit that generates clocks to be fed out to DRAM DIMMs.

Q. And I'm sorry. And what's a register?

A. A register was -- one flavor of DIMMs are referred to as register DIMMs, and what they do is they take some set of signals from the memory controller and they register them. That's a small component that consists of a series of flip-flops that register the

commands and then redistribute them on the DIMM to all the DRAM components.

Q. I'm not sure if this is a good question to ask, but what is a flip-flop?

A. Oh, boy. It's a basic state element that captures data and holds it.

Q. Now, why was the availability of the system components important to AMD's adoption of DDR?

A. It gets back to just because you have a DRAM doesn't mean you are able to build a computer. You need a lot of support components around it to make a fully functional computer and it's critical that in the commodity market you have multiple suppliers of all these components that all agree on the same specification and build compatible parts.

Q. Okay. Now, a couple of bullets, main bullets, below that you mention Rambus. You say, Rambus offered a complete system picture with RIMMs, clock chips, motherboard layout guides, I/O cell design, et cetera, and there was a committed system logic partner.

Now, what were you referring to there?

A. Rambus had done all of the work required to get systems put together. They had the motherboard design guidelines. They had a RIMM. They called it a

Rambus in-line module I believe. Instead of DIMM, it's RIMM.

But they had that standard. They had the layout done. They had the termination scheme specified. They had power supply components specified. They had clock chips specified. All of the support structure and components required to make a computer using Rambus technology, they had figured it all out.

Q. And you also say here "committed system logic partner." What was the importance of that?

A. That was obviously Intel had committed to including Rambus in their product line, and therefore, Intel was designing a chipset that would interface to Rambus, and given that there was a chipset manufacturer working on how to talk to Rambus that was driving a lot of the issue closure on the system-level solutions, so issues around pinout and layout and guidelines, et cetera, were obviously being worked with a committed system partner.

Q. Below that you say: "We realize that creating an S2K infrastructure was going to be tough enough. We really could not afford to create the DDR infrastructure at the same time."

I think you mentioned what S2K was earlier.

Could you remind me what that is.

A. So S2K was the term we used for the new K7 front-side bus, the new interface that we designed for K7 to talk to the rest of the system.

And many of the things I've been talking about, system-level components and design guidelines, a lot of that work had to be done also to get our partners enabled with the S2K. That was a new bus. It had new termination schedules, it had new layout rules, it required unique clock chips, layout design guidelines, and we had a team of folks that was working very hard to get all of our motherboard partners to implement the S2K properly in order for our microprocessor to work with that motherboard. It's almost exactly the same people that would have to be used to do the same thing for DDR if we chose to do that.

Q. So you were in the last part of your answer referring to the S2K infrastructure there?

A. Yes.

Q. Now, it says here that the IGR4 started in earnest in September 1998 after IG release. And IGR4 was what again?

A. IGR4 is the Rambus-compatible K7 chipset, Northbridge chipset.

Q. Now, in the next two bullets you describe the

work that AMD did with Rambus. The second bullet in particular says, "We worked closely with Rambus to use their RMC logic in the process, debugging numerous issues with RMC."

First of all, tell me, what does RMC mean?

A. RMC I believe stands for Rambus memory controller, and what it was was Rambus developed this chunk of verilog RTL code that implemented an abstract memory controller, the set of logic that you would want to design to be a memory controller for their Rambus device.

We quickly found out that it was not implementable. It was a very high-level abstract design, but when we tried to actually take this abstract and make a chip out of it, it wasn't very translatable, so we had to do a lot of work to make it implementable in a real chip.

In addition, when we started doing extensive simulation on the chip to verify its functionality, we discovered some bugs, a couple big ones, a lot of little ones, that were -- just had to be worked through, and there were questions on the exact protocol and the spec and a lot of interaction at the engineer-to-engineer level to get that right.

Q. Now, you mentioned the term "verilog RTL."

Just so I understand, what is verilog RTL?

A. Yeah. I apologize. That's a common programming language that chip designers use to design chips. It's the base design language of most chips these days.

Q. Now, next you say between the summer of 1997 and -- the summer of '97 and the fall of '98, JEDEC DDR turned around due mostly to the efforts of the folks at Micron who partnered with Micron PC folks to address the DDR system issues.

What are you referring to there?

A. Well, as I mentioned, what was missing in the whole DDR equation was a system partner that would drive all the system issues to get the layout, design guides, et cetera, put together. And it turned out that Micron had a division of their company that was developing PCs and chipsets, so they hooked up -- they, the DRAM Micron folks, hooked up with the Micron PC folks and started working out all these issues.

Apparently, the Micron PC folks designed a chipset, a DDR chipset, talked to an Intel microprocessor, but other than that, it was fine and it worked great with DDR. They built a motherboard, worked through the termination issues. They made a

DIMM layout that seemed to be pretty good, got some power supply vendors on board to develop power supplies that met some pretty reasonable specs, clock chips, et cetera. It seemed like they had the whole package sort of put together.

Q. Now, next you refer to a trip, AMD traveled to Micron PC in Minnesota.

Were you involved in that trip?

A. Yes.

Q. And what happened in that trip? First of all -- I'm sorry. I shouldn't have asked that.

Why did you go on that trip?

A. Well, we were invited by Micron PC -- by the Micron folks, both the DRAM and PC folks, to come see that DDR was real and that we should consider it for our future products.

So myself and Jim Keller, who at the time was the K8 processor architect, flew to Minneapolis and went and saw what Micron had done. We saw the motherboard. We looked at their layouts. We went into the lab and saw it working and put a scope on some signals and saw the pretty signal integrity and it was real, things were working well.

Q. And who at Micron were you working with on this?

A. The Micron DRAM person was Terry Lee and the Micron PC person was Joe Jeddlow, J-E-D-D-L-O-W.

Q. Next you say, "In parallel, lots of information from DRAM manufacturers on the real cost of DRAM."

Before we talk about the different information, what was the importance of receiving information from the DRAM manufacturers on the cost of DRAM manufacture?

A. The DRAM manufacturers are the final say in what it costs to manufacture their part. If you want to find out how good or bad a DRAM part is, you ask the DRAM manufacturer. They kept us up-to-date on what their costs were for various technologies moving forward.

Q. And why was it important for AMD to talk to the DDR manufacturers about the cost?

A. We needed to make sure that whatever memory we chose in our systems for our microprocessors was a commodity and met the performance requirements at the lowest possible cost.

Q. Now, some of the items listed below, let's go through some of those.

What was your understanding of the term "die area"?

A. What we were being told by the DRAM manufacturers was that comparing a like density DDR chip to a like density Rambus chip, the Rambus chip had larger die size. It was physically a bigger chip, which implied it was more expensive.

Q. Why does the larger size mean it is more expensive?

MR. GATES: Objection, Your Honor. It lacks foundation.

JUDGE McGUIRE: I can't hear you, Mr. Gates.

MR. GATES: It lacks foundation, Your Honor.

JUDGE McGUIRE: Sustained.

BY MR. DAVIS:

Q. Have you been involved in chip manufacture?

A. Yes.

Q. And in your involvement as a chip manufacturer, have you observed the importance of die size to the cost?

A. Yes.

Q. Okay. So could you answer what was the importance of die area.

A. The larger the die area of any semiconductor component, the higher the cost.

What you try to do as a chip designer, as a semiconductor manufacturer, is to have the absolute

minimum die size possible to meet your product requirements because there's only a certain number of die that fit onto a wafer and only a certain number of wafers that can go through a manufacturing facility in a given time period and that equals your -- that's the basis of your economic model.

Q. And test issues, what were you being told about test issues?

MR. GATES: Objection, Your Honor. It calls for hearsay.

MR. DAVIS: I'm not entering it for the truth of the matter but his state of mind in the decisions regarding the RDRAM chipset.

MR. GATES: If it's coming in under state of mind and not for the truth of the matter, I don't have any objection, Your Honor.

JUDGE McGUIRE: Noted.

BY MR. DAVIS:

Q. Do you have the question in mind? Do you remember the question?

A. No.

MR. DAVIS: Would you read back the question, please.

(The record was read as follows:)

"QUESTION: And test issues, what were you

being told about test issues?"

THE WITNESS: DRAM manufacturers were telling us that the Rambus devices required new, expensive testers and required longer test time than equivalent DDR devices.

BY MR. DAVIS:

Q. And why was that important to you?

A. Similar to the die size issue, the longer your test time, the higher your cost. You want to minimize your test time when you manufacture semiconductors. The longer you have to test a device, the less your throughput through your manufacturing line.

Q. The next item you have there is yield. What does that refer to?

A. That refers to after manufacture, whether a device meets its specifications or not. Devices that meet the specification are a yield, that's your yield, your positive yield, and the ones that don't are thrown away.

Q. And what were you being told about yield on this topic?

MR. GATES: Your Honor, it's again calling for hearsay. If it's coming in under state of mind, that's fine. I would just like to have a standing objection.

MR. DAVIS: And these questions will all be for the state of mind.

JUDGE McGUIRE: All right. So noted.

MR. GATES: Thank you.

THE WITNESS: So on yield we were being told that the Rambus devices weren't coming in as fast as they needed to be and therefore they were going to be quite expensive initially.

BY MR. DAVIS:

Q. The next item below that is power. What did that mean?

A. We were being told by the DRAM manufacturers that the Rambus devices were quite a bit hotter in operation than the comparable DDR device.

Q. And why is that important?

A. Higher power would imply higher cost in the system. A larger power supply and perhaps a heat sink to remove the power.

Q. And what were you being told about power by the DRAM manufacturers?

A. We were being told that the Rambus devices required heat sinks and the DDR devices didn't, implying that the Rambus devices would be more expensive.

Q. The next item below that is packaging. What

does that refer to?

A. We were being told by the DRAM manufacturers that Rambus devices required a new, higher-cost packaging mechanism -- I believe it was BGA -- whereas the comparable DDR devices were still being packaged in the current-generation package technology. I believe it's referred to as TSOP, T-S-O-P.

Q. And why was that important?

A. Again, BGA was more expensive than TSOP.

Q. And I'm sorry. Did you say what you were hearing from the DDR manufacturers?

A. Yes. This is all what the DDR manufacturers were telling us.

Q. And the final item there is RIMMs, and it's capital R-I-M-M-S, all caps up to the last M. Sorry.

What does that refer to?

A. A RIMM is the term that Rambus coined for their memory module, their -- analogous to the DIMM. Rambus in-line memory module I believe is what it stands for.

And in the context of this statement, what the DRAM folks were telling us is that the RIMMs were hard to manufacture because of the yield issues and the test issues. They had to do a lot of testing after the devices were assembled onto the RIMM itself, and

therefore, if they found a bad component out of the multiple components on a RIMM, they'd have to throw the whole RIMM away or rework it, which is just adding cost, large amounts of cost, to the actual RIMM manufacture process.

Q. And why was that important to AMD?

A. Again, we needed to make sure that the memory required for use with AMD microprocessors was cost-effective and commodity, widely available at the lowest possible cost.

Q. The next bullet refers to future K8 implementations. K8 again was -- what was K8?

A. K8 was our next-generation microprocessor, sometimes referred to as Hammer.

Q. And then you say here "It became clear WRT," does that mean with respect to?

A. With respect to, yes.

Q. The difficulties of getting a Rambus controller on die.

What are you talking about there?

A. Here, I think I referred to previously that our memory controller for K8 we decided to integrate onto the microprocessor die itself. Traditionally, memory controllers are implemented in the Northbridge chipset, a separate chip from the microprocessor, and there's

some fundamental differences between the semiconductor processes used for the manufacture of chipsets and the semiconductor processes used for the manufacture of microprocessors.

With chipsets, the goal is lowest possible cost with a constant control of the process technology so that when you start manufacture of your Northbridge chipset, you assume that the semiconductor process technology parameters aren't going to move around over the lifetime of the product. That product will remain stable.

And that's particularly crucial in Rambus with their rack design. As I referred to earlier, the rack is their sophisticated I/O cell design that has a lot of very detailed analog, careful analog design, that depends upon, critically upon stable semiconductor process technology parameters. That works well and when the Northbridge -- the memory controller is implemented in the stable process technology such as, you know, the ones from UMC or TSMC.

On the microprocessor side, it's a completely different equation. The way microprocessor semiconductor process technology is targeted, you tape out the microprocessor initially and then you're constantly tweaking the process technology to ever

increase the speed of that microprocessor over its lifetime.

If we had decided to implement the Rambus memory controller on the microprocessor using the microprocessor semiconductor technology, we would have been constantly tweaking and constantly having to tape out new versions of the microprocessor to adapt to the changing process technology underneath it in order to keep that rack cell working.

The rack cell is quite dependent upon --

JUDGE McGUIRE: Okay. I'm not going to let him just go on and on. I understand what you're trying to say, sir, but let's ask more tighter questions so we don't have four or five pages of narrative, if you would.

MR. DAVIS: That was my fault, Your Honor. I'm sorry.

BY MR. DAVIS:

Q. Just so I understand it, AMD had made a decision not to use RDRAM with the K8; is that accurate?

A. That was the direction at that time, yes.

Q. Did that decision have any effect on the decisions that were made regarding the K7?

A. Yes. We wanted to make sure that when we

had -- when we introduced K8 with DDR that we had an established infrastructure for DDR, and a good way to do that would be to introduce a DDR chipset for K7.

Q. The next item refers to a complete design team freed up in AUS. Does that refer to Austin?

A. Yes.

Q. And what's that item in parentheses that says "EPD"?

A. Embedded products division, which was a division that more or less went out of business at about that time.

Q. Now, what was the importance of the design team being freed up in Austin?

A. That team could be applied to doing a parallel chipset effort, and in fact we let -- asked them to take on the task of designing a DDR version of the K7 chipset.

Q. Okay. Now, one item below that, you say, "Due to resource constraints and continuing bad news about RDRAM in April 1994, IGR4 was put on the shelf with full intentions to restart later."

What was the bad news that you were referring to here?

A. There started to be industry rumors, industry articles about problems with Rambus. The Intel

Northbridge -- I believe that's what the IA20 refers to -- the Intel chipset that was designed to work with Rambus was delayed a number of times in its launch. Sort of the bad news that the DRAM folks were telling us prior to then started to become public based on the attempt by Intel and Rambus to get that technology ramped into the production.

Q. What was the importance to AMD of the bad news you referred to with respect to the IA20?

A. It implied that there were problems getting this technology to market and it supported the statements that the DRAM folks were telling us that it's going to be more expensive than DDR.

Q. Okay. Now, the last bullet in the document says, "General sampling of IGD4-based motherboards to DRAM manufacturers started in March of" -- I guess that's 2000? Is that accurate?

A. Yes.

Q. When did production of IGD4-based motherboards begin?

A. I believe it was either September or October 2000.

Q. Why did it take from March of 2000 to September or October of 2000 to go from general sampling of IGD motherboards to production?

A. We had to make sure that all of our partners designed the motherboards properly, that all of the DRAM DIMMs that were manufactured by all our partners worked properly, a big qualification, making sure all the DRAM devices and all the DIMMs worked interoperably with the different motherboards that were all designed to work with IGD4.

At the same time, we had a few bugs towards the end of, you know, the end of the summer getting that into production. It's the general ramp-up to production.

MR. DAVIS: Now, I understand that this has already been moved into evidence. If it hasn't, I would move it in, but I understand it has been.

JUDGE McGUIRE: And if it has, then it's not pertinent that it be now moved.

MR. DAVIS: Okay. I'll move it in later.

JUDGE McGUIRE: I'm trying to be -- it has been moved into evidence already; is that correct?

MR. GATES: Your Honor, I believe it was moved in on Friday. I just don't have my list here.

JUDGE McGUIRE: But we aren't sure?

MR. DAVIS: No. I understand that it was.

JUDGE McGUIRE: It was or was not?

MR. DAVIS: I believe it was.

JUDGE McGUIRE: Well, in case it hasn't been, is there any objection?

MR. GATES: There's no objection.

JUDGE McGUIRE: Then if not, it will be entered if it hasn't already been entered.

MR. DAVIS: Thank you, Your Honor.

JUDGE McGUIRE: Thank you, Mr. Davis.

BY MR. DAVIS:

Q. Are you aware of an organization known as JEDEC?

A. Yes.

Q. When did you first become aware of JEDEC?

A. When I was at Apple, the procurement folks updated us periodically about the ongoing industry situation and JEDEC was mentioned.

Q. Do your current job duties involve JEDEC in any way?

A. Yes. The AMD representative to JEDEC works on my team.

Q. Who is that?

A. That's Sam Patel.

Q. Could you tell me what JEDEC is.

A. It's an industry consortium that defines standards that multiple manufacturers can design to to have interoperable parts.

Q. Have you ever gone to a JEDEC meeting?
A. I've been to a few. Yes.
Q. How many, approximately?
A. Maybe three or four of them.
Q. Why did you go to the JEDEC meetings?
A. I go to back up Sam when he needs extra help. There's usually a lot of issues that occur during a JEDEC meeting. They take a week, but they try to pack two weeks' worth of work in and there's a lot of sidebar conversations, a lot of issues to address, and when those issues become overwhelming for one person, I go to support Sam.
Q. What is your understanding of the importance, if any, of the JEDEC standards to AMD's business?
A. AMD views the JEDEC standards process as crucial to its business. JEDEC allows manufacturers to all design to a common standard and basically enables the commodity marketplace. Everybody is designing compatible parts at the lowest possible cost competing on manufacturing cost.
Q. I'd like to show you a document that's been marked for identification as RX-1839.
A. Yes.
Q. Do you recognize this document?
A. Yes.

Q. What is it?

A. It's an e-mail trail, set of exchanges, where I was preparing for a participation in a panel discussion at a VLSI symposium in Japan scheduled for June 2001.

Q. What was the VLSI rump session that's referenced in the subject line?

A. The VLSI symposium is this big conference of all the VLSI designers, VLSI semiconductor designers, in the world and they have day-long sessions of very boring, highly technical presentations, and in the evening they had some panel discussions, and the request was to have a lively panel discussion about DRAM and they asked various people to represent different technologies and encouraged a lively discussion.

Q. What do you mean, "a lively discussion"?

A. Controversy. Conflict. They wanted to put a little juice in the proceedings from a day-long, boring semiconductor discussion to a lively presentation in the evening to keep the engineers entertained I guess.

Q. And the presentation that you have in the back is the presentation of that?

A. Yes.

Q. In the last paragraph, I guess the second to last full paragraph, it's the one starting "Are DDR memory controllers," there's a sentence that says, "Alternate memory technology interfaces use roughly 65 percent of the memory controller resources that a typical 64-bit DDR interface requires."

What is that referring to?

A. There were questions -- I don't honestly remember the source of the questions, but there were questions related to, gee, Rambus only requires, you know, some number of pins and DDR requires a larger number of pins, doesn't that mean that Rambus is less expensive to implement. And this paragraph explains my response that it's -- you just can't count pins to get your cost. There's other issues to think about.

Q. In fact, the next sentence says, "However, saving a few pennies in the memory controller while spending quite a few dollars in other parts of the system" -- and then there's a parenthetical there -- "is not the right trade-off."

And what were you talking about there?

A. At that point in time the -- our understanding was that Rambus required -- implementing Rambus technology in the motherboard required six-layer motherboards. There were heat sinks attached to the

Rambus. There's -- the sockets for Rambus were quite expensive compared to DDR at that point. The same thing goes for the regulators and clock chips. They hadn't achieved the commodity price point yet. In addition to the basic cost issues of the device itself that we talked about earlier.

Q. The next sentence starts, "AMD believes that the sweet spot for mainstream memory controller technology," and it goes on from there.

What do you mean by "sweet spot"?

A. Our Chinese partners who develop chipsets and motherboards had -- were very familiar with given size packages and layout rules, four-layer motherboards, et cetera, that we believed that the DDR requirements matched that very well, whereas the RDRAM requirements did not.

Q. Okay. At the bottom of the next page, there's an e-mail that I believe is from you and if you could confirm this.

A. Yes.

Q. So starting with the -- it says "original message"?

A. Yes.

Q. Is that -- so is the text underneath that, the last original message, is that something that you

wrote?

A. Yes.

Q. The very last line says, "JEDEC is a pain."

What did you mean by that?

A. JEDEC is open to any and all parties, so any and all parties have an opinion and can contribute or delay, or everybody has a vote, so it's not always the most straightforward thing to get a technical specification through. It's sometimes long, laborious, and you have to argue your points endlessly, probably much like Congress down the road, but it's successful and it works.

Q. And after that, you say, "But evolutionary gets you incremental performance gains sooner."

Sooner than what?

A. Sooner than a revolutionary change, that you can make minor modifications to an existing spec to get more performance. That happens a lot easier and quicker than to throw the whole design out and start over with something brand-new to get a little bit more performance. You can just start tweaking the design a little bit over time to get your performance increase, and that's a much quicker way to get performance increases than throwing everything out and starting over again.

Q. I'd like to point you to the last -- I believe it's the last three pages of the document.

A. Is that the actual presentation?

Q. Yes, the very last -- the last three pages starting with the third from the end.

A. Okay.

Q. Which is actually page 7 of the document.

A. Okay.

Q. What are these slides?

A. These are the slides that I presented to start out the panel rump session. They asked us to have a few slides, speak for five minutes to give a base opening presentation of what our position was, whatever technology we were advocating.

Q. And who put these slides together?

A. I did.

Q. Were these the slides that were used at the session?

A. Yes.

Q. A few bullets down there's an item that says "die and controller flexibility."

What did you mean by that?

A. DDR technology allowed both DRAM components and memory controller components to have -- to implement both the old single data rate or a PC100/PC133 spec and

with the same component also implement the DDR spec, which would allow backwards compatibility, and in fact I believe most of the first DDR DRAM devices were in fact dual mode. They could work in single data rate mode and become a PC100 product or they could work in DDR mode and be a DDR product.

Similarly, a number of our chipset partners did the same thing with their chipsets. They made memory controllers that could work with either a single data rate or double data rate.

Q. The title of this slide is System Advantages of DDR.

Why is die and controller flexibility an advantage to DDR?

A. It allows for evolutionary change. It allows for a crossover period in technology when -- technologies don't just you obsolete one and you come out with a brand-new one overnight. There's a ramp. The old technology ramps down slowly; the new technology ramps up slowly. In that crossover period it's typically painful to keep your business running. It's hard to predict the adoption rate of the new technology.

By allowing this flexibility, manufacturers could adapt to what the market demanded. If the

market demanded more single data rate in lower-cost markets, they could supply that. If the market demanded the DDR versions, they could supply it with the same device.

Q. Now, earlier you had stated that AMD designs and sells controllers sometimes?

A. Yes.

Q. Does it generally make them work with both DRAMs and a transition, technology transition?

A. We close not to for our IGD4 device. When we started the design of that, we decided to focus on getting the DDR infrastructure going with our IGD4 device, get it out there as soon as possible with the lowest risk. Adding an SDR certainly would be possible, maybe even straightforward, but it added risk, but it added not trivial schedule. We decided to go out and get DDR going, get the infrastructure going, get the industry going.

Q. Okay. Let's go to the next document.

Do you know whether it matters to AMD whether or not the DRAM standard or a DRAM standard is generated inside of JEDEC or inside -- instead of inside a smaller consortium or industry group?

A. As long as it's an open, free consortium where all interested parties are able to contribute, it's

fine with us. Generally, that means JEDEC.

Q. Has there been a situation in which a DRAM standard was developed or was in the process of being developed outside of JEDEC?

A. Yes.

Q. And what examples are you referring to?

A. Well, there was ADT and Rambus.

Q. What is ADT?

A. ADT I believe stands for Advanced DRAM Technology. I believe it was a consortium of a handful of the DRAM manufacturers and Intel who were defining some next-generation DRAM technology.

Q. Were you involved in AMD's business plans regarding DRAM when the ADT standard was being developed?

A. Yes.

Q. Did you have any understanding of the effects such a standard would have on AMD's business?

A. Yes. We were very, very afraid of what it would do to our business. Our number one competitor was essentially defining the new DRAM standard, getting a huge head start in its implementation and details, designing for its requirements without any input from AMD.

Q. I'd like to show you a document that's been

marked for identification as RX-1746.

Do you recognize this document?

A. Yes.

Q. If you'd refer to the top e-mail of the string, you state, "I want to make sure we send a clean, strong message to our DRAM partners that we will not tolerate any spec changes that are not approved through JEDEC."

What are you referring to in this sentence?

A. We had become aware of some changes to the DDR device specification that Intel was attempting to make outside of JEDEC. I believe they were going directly to the DRAM manufacturers and asking for this spec change.

Q. And what do you mean by "spec change"?

A. Device parameters, specs are -- can encompass a wide range of things. I believe in this case it was some timing specifications that were being suggested as Intel wanted to change them.

Q. And why was it so important to you that the spec changes get approved through JEDEC?

A. Again to make sure that all interested parties had a chance to contribute and to make their opinions and needs known. With just Intel driving, we didn't know -- we didn't know what the spec changes were and

whether that would affect us or not and how it would affect us.

Q. Okay. Do you know what DDR 333 is?

A. Yes.

Q. What is it?

A. It is the follow-on to the original DDR 200 and 266 speed specifications, sometimes referred to as DDR 1.5, but it's an evolutionary speed increase in DDR.

Q. Are AMD processors compatible with DDR 333?

A. Yes.

Q. Which processors are compatible with DDR 333?

A. Our K8 microprocessor. It's commonly referred to as Opteron now that we've launched it.

Q. I'd like to show you a document that's been marked for identification as CX-2152.

Do you recognize this document?

A. Yes.

Q. What is this document?

A. This is a -- I believe this is a meeting minutes write-up that I wrote after a meeting.

Q. I'm sorry. You said you wrote this?

A. Yes.

Q. The first paragraph -- well, first of all, it says "IGD4 Based DDR 1.5 Summary," so what was being

discussed in this meeting?

A. We were discussing the feasibility of adding DDR 333 support to our existing IGD4 part that was at that point I believe starting production.

Q. And the first paragraph describes a PPP meeting. What does that stand for?

A. Yeah. PPP stands for propeller head platform planning. It's a weekly meeting that is held at AMD that I chair that's a cross-divisional lead engineer/senior engineering discussion group.

Q. Okay. Now, what was the time frame in which -- who was requesting, first of all, that IGD4 be able to support DDR 1.5?

A. Our marketing team at AMD asked for it.

Q. In what time frame were they hoping to see this product?

A. I believe they were hoping to have a product in the market in mid-2001.

Q. What did you do to provide the analysis that's described in this memo?

A. We asked the design team, the IGD4 design team, to go off and figure out what it would take to modify the design to support DDR 333.

Q. I'd like to direct your attention to the item in the memo entitled What Are the Constraints,

Obstacles, Risks, et cetera, to this Project? Do you see that?

A. Yes.

Q. Could you identify or -- sorry -- could you describe what you identified as the constraints related to the project?

A. So typical engineering practice is when you're asked to do something challenging, you want to constrain the problem down to the minimum set of things to solve, so we put some constraints and said, well, we're going to only do this for registered only with two DIMMs and we're not going to entertain other feature additions to the part. We want to narrow the focus of the problem we're trying to solve.

Q. Can you describe what you identified as the risks related to the project?

A. The biggest risk was that we had other projects in the pipeline that were slated to use the resources that would be needed to make this change to the chip.

Q. It says "imposes risks to tunnel projects"?

A. Yes. That's what that refers to. The tunnel is what we refer to as the chipsets for K8.

Q. Is that similar to bridge?

A. Yes. For K8 we changed the system

architecture radically, as I discussed, to pull the memory controller on the processor, and to make sure everybody wasn't confused, instead of calling things Northbridge and Southbridge, we called them tunnels. A tunnel does the same thing as a bridge, but it's constructed radically different, so it got the point across.

More geeky engineer stuff here. Sorry.

Q. Could you identify what you described here as the obstacles related to the project.

A. The biggest obstacle -- I think they're detailed a little bit later, but the biggest obstacle was we needed to make some changes inside the IGD4 part itself. The current part had the frequency of the DRAM in locked step with the frequency of the front-side bus. If the front-side bus was going at 266 megahertz, the DRAM would go at 266 megahertz.

By asking us to go to 333 megahertz memory, we would have to put some sort of gearbox structure inside the chip to adopt the different clock speeds.

Q. What do you mean by the term "gearbox"?

A. We would have to make sure that as data went across the chip from the K7 front-side bus side up to the memory it had to change time demands from a 266-megahertz time demand up to a 333-megahertz time

demand. And that required a bunch of logic that wasn't in there. It wasn't in the chip.

Q. You also mention here that there were DDR infrastructure issues that were involved as obstacles.

What were you referring to there?

A. We believed at the time that there needed to be a new DIMM qualification for the faster DIMMs, for the faster devices. And that would be a set of work that had to be done.

MR. DAVIS: I'd like to move Exhibit 2152, CX-2152, into evidence.

MR. GATES: No objection, Your Honor.

JUDGE McGUIRE: So entered.

(CX Exhibit Number 2152 was admitted into evidence.)

BY MR. DAVIS:

Q. Did you at some point become aware that Rambus claimed patent rights over some of the technologies used by AMD in some of their products?

A. Yes.

Q. In about when did you find this out?

A. It was late summer 2000 I believe.

Q. And how did you find this out?

A. One of my bosses gave me a set of patents and asked me to look at them.

Q. And what was the nature of the analysis that they asked you to perform on those patents?

A. They wanted to see, A, if we were in violation or did we, you know, did we infringe on the patents, I guess is the right word, and B, were there any reasonable work-arounds.

JUDGE McGUIRE: Now, let me interject. When you say your boss handed you some patents, whose patents were these? Rambus patents?

THE WITNESS: Yes, they were Rambus patents.

JUDGE McGUIRE: All right.

MR. DAVIS: Thank you, Your Honor.

BY MR. DAVIS:

Q. Were you aware of what technologies Rambus claimed AMD was using that infringed their patents?

A. Yes. There were four basic patents that I looked at. There was one on dual-edge clocking, there was one on programmable CAS latency, one on programmable burst length, and the fourth one had to do with a DLL and a DRAM. I didn't look at the fourth one. DLLs aren't my expertise.

Q. Do you know which AMD products were affected by these claims?

A. I was told to look at them for both our existing IGD4-based product, our K7 chipset products,

and the future K8 microprocessor.

Q. At what stage was that future microprocessor -- this is the K8 you said?

A. Yes.

Q. And what stage was the K8 at at the time you learned of the Rambus claims against AMD?

A. It was about midway through its design cycle. Its base architecture was defined. It was well into the design phase. It hadn't quite reached the phase of physical design, but it was well along the path to completion.

Q. Now, you said you reviewed the Rambus patents or three of the Rambus patents?

A. Yes.

Q. Now, what did you conclude after reviewing the patents?

A. They were pretty simple things to work around if we had known about them a long time ago, but we were in the middle of ramping up an infrastructure. This was just when we were trying to get our IGD4 and the first DDR motherboards out the door. They were pretty trivial to work around, but we were in the middle of ramping and they're pretty tough to change things.

Q. What was the importance of being in the middle

of ramping to the issue of working around the Rambus patents?

A. The work-arounds that were obvious required some big changes to the device, to the chipsets, to the motherboards, et cetera.

Q. What work-arounds were you referring to?

Start with programmable CAS latency. What work-arounds did you have in mind in this analysis?

A. There were any number of options. The bottom line is any change when you're trying to do a production ramp is extremely difficult and hard, so you asked about programmable CAS latency; correct?

The few work-arounds we talked about were --

MR. GATES: Your Honor, can I interject here an objection? I think there's a lack of foundation and we're just getting opinion testimony at this point.

MR. DAVIS: This is not opinion testimony. This is his state of mind in 2000 when he learned of the patents, but I can establish a foundation if you like.

JUDGE McGUIRE: Overruled. I'll entertain the question.

BY MR. DAVIS:

Q. Do you remember the question?

A. What work-arounds were we contemplating.

Q. For programmable CAS latency.

A. For programmable CAS latency.

So the three on the table were pretty obviously how to fix CAS latency, have the parts manufactured to be a fixed CAS latency. The second one was to have a pin-programmable CAS latency where the value of CAS latency would be set by pins tied high or low on the DIMM. And the third one was some sort of serial programming using existing single-bit serial load technology that was ubiquitous in the industry at the time.

Q. So let's talk about pin strapping for a second.

What did you mean by pin strapping?

A. With pin strapping one could allocate either dedicated or multiplexed pins on the DRAM device that depending on their state either pulled high or low would tell a device what the CAS latency should be.

Q. Now, when you say "pulled high or low," what are you referring to (indicating)?

A. Pulled to a high voltage to indicate a one or pulled to a low voltage to indicate a zero.

Q. Did you think that pin strapping was a more costly or less useful future than the current JEDEC

standard of setting CAS latency?

A. Certainly no more costly. Maybe a little bit more inconvenient, but in the end it probably could have been made to work just fine. The problem was, we'd have to change everything in the middle of this production ramp.

Q. What about fixing CAS latency?

A. Fixed CAS latency would have been pretty onerous for the DRAM manufacturers.

Q. Let's -- first of all, did you think that fixing CAS latency was more costly or less useful than the current JEDEC standard to AMD?

A. Probably it had -- would have a significant cost impact for the DRAM manufacturers.

One of the advantages of programmable CAS latency is that DRAM manufacturers can bin their devices. They can have fast devices with a short CAS latency and sell them for more money, and parts that were perhaps yielding slower, they could be programmed with a longer CAS latency and sold for less cost.

Q. Now, I forget -- did you remember the name of the person who gave you the patents and the assignment?

A. It was either Rich Heye or Dirk Meyer. I forget exactly which one.

Q. Did you recommend to either of them that AMD change its products to change the CAS latency that it used?

A. No. I recommended we didn't, given that we were in the middle of our production ramp. It would have caused a big -- a big hiccup.

Q. Now, what was your understanding of the term "programmable burst length"?

A. I'm sorry. I didn't hear.

Q. What was your understanding of the term "programmable burst length"?

A. Programmable burst length allows the DRAM devices to either send four cycles of data back for a burst and/or eight cycles of data with a burst command.

Q. And what were the alternatives that you had in mind in 2000 when you reviewed the Rambus patents?

A. For work-arounds?

Q. Yes.

A. Very similar to the CAS latency work-arounds. Fix the burst length, use pin strappings or a serial load technique.

Q. Did you also consider fixing the burst length?

A. Yes.

Q. What was your analysis of fixed burst length as

it relates to AMD's business?

A. Fixed burst length would have been very, very bad for AMD. AMD designed its microprocessors to have its natural burst length to be 64 bytes, which is eight cycles of data. Knowing that the DRAMs had that capability, we decided to take advantage of that capability for performance reasons.

If the work-around was to fix the burst length, the most likely burst length chosen would have been an Intel-compatible burst length or a burst length of four cycles or 32 bytes. That would have been very bad for us. A, it would have required lots of redesign in the memory controllers and also caused us a performance hit.

Q. Now, why did you say that you thought that the most likely burst length would have been the -- you said burst length of four?

A. Yes.

Q. And why did you think that would be the most likely burst length that would have been used?

A. That is the burst length that Intel uses for their microprocessors and their systems and they hold the majority of the market and the DRAM manufacturers would have manufactured the part to hit the majority.

Q. I understand.

The last technology you would have added, is that dual-edged clocking?

A. Yes.

Q. And what is dual-edged clocking?

A. Dual-edged clocking allows data to be captured on both a rising edge of a clock and the falling edge of the clock. Traditionally, prior to -- I don't know -- the mid-'80s, data was always transferred on a single edge, on the rising edge of the clock. Data was captured when the clock rose from a zero to a one.

DDR techniques allowed you to capture the data on the falling edge and the rising edge to effectively double the data rate, hence the word "double data rate" or "DDR."

Q. What were the alternatives that you had in mind in 2000 when you reviewed the Rambus patents regarding dual-edged clocking?

A. Well, the placement of your clock edges and your data is more or less arbitrary. We could have slowed the clock down by half the rate or doubled the rate of the clock itself. Either way would have been reasonable to implement to capture the data.

Q. Did you propose to Mr. Heye or Mr. Meyer or whoever gave you the patents that AMD change its products to accommodate changes to the dual-edged

clocking?

A. I recommended that we wouldn't make any changes for similar reasons as before. We were in the middle of a production ramp. It would be impossible for us to stop and change.

Q. Now, earlier you were describing an analysis in CX-2152, which is -- (indicating).

A. Yep.

Q. What was the date this analysis occurred? What was your understanding of that?

A. The date on the document says June 29, 2000. It probably occurred the previous couple of weeks to that date.

Q. And how does that relate in time when you learned about the Rambus patents, the Rambus -- I'm sorry -- the Rambus claims against AMD?

A. This preceded that, that knowledge.

Q. Is there any difference between the analysis you conducted here and the analysis that you conducted relating to the patents that Rambus showed you -- I'm sorry -- that Rambus claimed against AMD?

A. Yes. Here was a very straightforward incremental speed increase and I had the design team look at what it would take.

For the work-arounds that we were previously

discussing, I communicated with a few of our DRAM partners and a couple of senior folks inside AMD. I didn't go to any team and ask them to do a detailed analysis. It was a very top-level lead work, very simple changes that -- you know, the work-arounds that we talked about were very simple in concept and the reason -- the reasons around doing them are not -- didn't surround the technical feasibility. It surrounded the logistical nightmare of trying to change something in mid-production.

MR. DAVIS: Thank you. No more questions.

JUDGE McGUIRE: Okay. Why don't we take a ten-minute break and when we return we'll start with cross-examination.

We're in recess. Off the record.

(Recess)

JUDGE McGUIRE: Mr. Gates, at this time I'll entertain your cross-examination of the witness.

MR. GATES: Thank you, Your Honor.

CROSS-EXAMINATION

BY MR. GATES:

Q. Good afternoon, Mr. Polzin. How are you?

A. Hi, Sean.

Q. You said earlier that you helped design the front-side bus for the Athlon processor; is that

right?

JUDGE McGUIRE: Mr. Gates, I'm going to ask you to stand a little closer to the mike. I'm having a little trouble hearing you from that far away.

MR. GATES: Okay. Thank you.

JUDGE McGUIRE: Thank you.

THE WITNESS: Design a bus.

BY MR. GATES:

Q. Well, let me ask you --

A. Yeah. Ask a different way. I'm sorry.

Q. You were involved in a team that worked on the Athlon processor; right?

A. Yes. I worked on the Northbridge chipset that interfaced to it.

Q. And you said something about it was a unique front-side bus with that Athlon chip; is that correct?

A. Correct.

Q. And when it first came out, it was -- I think you said it was operating at 200 megahertz; is that right?

A. Yes.

Q. Now, what I want to do is try to get some dates because the speed of that bus changed over time; isn't that right?

A. That's correct, yes, it did.

Q. It went from 200 and later on you got a faster bus?

A. Yes.

Q. And I think at one time you had a 333-megahertz bus; is that right?

A. Yes.

Q. Well, let me try to get some dates on these changes.

Okay. So the AMD Athlon, that's the K7; is that right?

A. Yes.

Q. And you said the front-side bus speed when it first came out was 200 megahertz; is that right?

A. Yes.

Q. Okay. And you said you worked on the chipset for that initial version of the K7?

A. Yes.

Q. And the initial chipset that came out with K7 was the AMD 750?

A. That's correct.

Q. Okay.

A. I referred to that previously as Irongate. If that helps.

Q. Okay. Or Irongate.

And when was that -- when did that chipset come

out, what year was that?

A. In June 1999 when we launched the first K7.

Q. And what type of memory did that chipset operate with?

A. PC100.

Q. Okay. So it's PC100 SDRAM?

A. That's correct.

Q. And we'll say that's 6-99; is that right?

A. Yes.

Q. Later on, you developed at AMD a faster front-side bus, 266 megahertz, for the Athlon chip; is that right?

A. Yes.

Q. And you worked on the controller that would go with that new front-side bus; is that right?

A. No. At that time a different design team was working on that.

Q. Okay.

A. I was the system guy at that point.

Q. You were the system guy at that point.

Did it have a different controller than the AMD 750?

A. Yes.

Q. And that was the AMD 760?

A. Yes.

Q. And when did this front-side bus come out?

A. September 19 -- or September 2000. That's the -- it was coincident with the introduction of the AMD 760 which was our IGD4 chipset.

Q. And that AMD 760 chipset was compatible with what memory technologies?

A. DDR 200 and 266.

Q. Now, did you ever develop a chipset that was compatible with PC133 SDRAM?

A. No.

Q. Third-party vendors created chipsets that were compatible with PC133 and the AMD processor; is that right?

A. Yes.

Q. Were they compatible with the 200-megahertz front-side bus or the 266-megahertz front-side bus?

A. I believe they were compatible with the 200, but I don't know for certain if they ever were not compatible with the 266. They may have been; they may not have been.

Q. Do you know whether or not those chipsets came out in between the AMD 750 and the AMD 7 -- the AMD 750 and the AMD 760?

A. I believe they do. I don't have any direct knowledge. I can't give you a date.

Q. Okay. So at some point third-party vendors came out with chipsets compatible with the Athlon that operated with PC133?

A. Yes.

Q. And we just don't know the date?

A. Yeah.

Q. Now, is the architecture of the AMD 760 chipset different from the AMD 750?

A. Architecture. Could you explain what you mean by "architecture."

Q. Well, what are the differences between the 760 and the 750 chipsets in very general terms?

A. In general terms, the 760 implements DDR memory. Its memory controller is different, and it also implements 4XAGP graphic support, whereas the 750 was the first-generation AGP graphic support.

Q. You could not use the SDRAM PC100 or PC133 with an AMD 760 chipset, could you?

A. That's correct.

Q. So it wasn't -- and you could not use a DDR with the AMD 750 chipset?

A. That's correct.

Q. So those are not backward compatible; is that right?

A. The chipsets were not. That wasn't their aim.

That wasn't their goal. That's correct.

Q. Later on, AMD developed a 333-megahertz front-side bus for the Athlon processor?

A. That's correct.

Q. And do you know when that came out?

A. I really have no idea.

Q. Were you aware of it when it came out?

A. Yes.

Q. Okay. So at some point you knew what the date was?

A. Yeah. I just don't recall when it was.

Q. Would it refresh your recollection if I showed to you a press release of when that chipset was released?

A. Sure.

Q. Then why don't we bring up on the screen AMD 04. I'll go ahead and give you a paper copy as well so that you can see that and it's probably easier to read.

May I approach, Your Honor?

JUDGE McGUIRE: Yes, you may.

MR. GATES: Thank you.

BY MR. GATES:

Q. Okay. If you could highlight -- bring up the first paragraph where it says "Sunnyvale."

Okay. Do you see the first paragraph where it says "Sunnyvale, California, October 1, 2002"?

A. Yes.

Q. And go ahead and read that paragraph to yourself.

Does that refresh your recollection of when it was that AMD introduced the Athlon chip with the 333-megahertz front-side bus?

A. That's correct. Yeah.

Q. So the date here, October 2002, is consistent with your recollection of when that was released?

A. Yes.

Q. And what type of memory was the 333-megahertz front-side bus compatible with?

A. Reading down further, it says it's compatible with DDR 333.

Q. Is that consistent with your recollection?

A. Yes.

Q. Okay. And do you know, did AMD develop a chipset that was compatible with DDR 333?

A. No.

Q. So third parties created a chipset for that particular type of memory?

A. Yes.

Q. Later on, didn't AMD develop an even faster

front-side bus for the Athlon chip?

A. Yes.

Q. 400 megahertz?

A. Yes.

Q. And do you remember when that was released?

A. Very recently. I know that. I don't have the precise date, but it was within the last couple months.

Q. So in about May of this year; is that --

A. Yeah. Sounds about right.

Q. And what type of memory is that 400-megahertz front-side bus compatible with?

A. I believe it's 200, 266, 333 and 400.

Q. So it can go with any of the DDR family up to DDR 400?

A. I believe so, yes.

Q. And did AMD develop a chipset that was compatible with DDR 400?

A. Not for K7, no.

Q. Not for the K7?

A. Yeah.

Q. So that was developed by third parties?

A. Yes.

Q. Now, we looked earlier at a document that you should still have. I think it's CX-2152. It's the one

with the copy of this slide in the binder and it has a discussion of DDR 1.5?

A. Yes.

Q. And that was a discussion of building a chipset that would be compatible with DDR 333; right?

A. Yes.

Q. In order to do that, at least with the slower bus speed, you had to rearchitecture the Northbridge; right?

A. Correct.

Q. And wasn't the case that there were different DIMM specifications for the DDR 333 than there were for the previous generations of DDR?

A. Different DIMM specifications.

Q. Well, let's look at this document on page 3. If you'll look at the third page, and if you look under -- there's a heading DDR Infrastructure Issues and Tasks?

A. Yes.

Q. If you look at the fourth bullet point, the third and fourth bullet points, it says that there's no device specifications available and later on it says "no DIMM layout available." Do you see that?

A. Oh, yes. Okay. Okay.

Q. So do I understand that correctly to mean that

there is a different DIMM specification for DDR 333 products?

A. Well, at this point in time it was not known whether the existing one would work fine or whether a new one was required.

Q. Well, isn't it -- later on isn't it in fact the case that there was developed a different specification for the DDR?

A. I believe you're correct.

Q. Okay. Are you familiar with a -- something called a Hot Chip Symposium?

A. Yes. Isn't that the one that happens in Stanford once a year? Okay. Yes.

Q. And didn't you give a presentation at the Hot Chip Symposium in 1999?

A. Me personally or me, AMD?

Q. You as part of a group from AMD.

A. I don't recall. I don't think I attended.

Q. Did you ever give a presentation on the IGR4 that you were developing at AMD to a symposium?

A. I don't believe I did, no, not personally.

Q. But do you know whether or not anybody from AMD did that or not?

A. I have no knowledge one way or another. They might have.

Q. Now, you spoke earlier about the importance to -- of JEDEC to AMD?

A. Yes.

Q. And I think you said it was important that it was an open process, everyone could be involved; right?

A. Yes.

Q. And the reason why it's important for AMD to be participating in an open process is so that you don't get a competitive disadvantage to Intel; is that right?

A. That's one of the reasons, yes.

Q. And that's one of the reasons why you were very concerned about the ADT consortium?

A. Yes.

Q. Because AMD was not participating, but Intel was?

A. Yes.

Q. We looked earlier at an e-mail that you sent. It's RX-1746. It's just a one-pager.

A. Okay.

Q. Okay. And this was an e-mail that you wrote in response to something that Intel was doing; right?

A. Yes.

Q. And they were specifying in an addendum

something additional to the DDR DIMM specification?

A. Yes.

Q. And you were concerned about that because it might put AMD at a disadvantage?

A. Yes.

Q. And you wanted to make it clear to your DRAM partners that you wouldn't -- AMD would not tolerate that type of behavior?

A. Yes.

Q. And you referred to that as borderline antitrust territory?

A. That's what it says here, yeah.

Q. Okay. Now, isn't it a fact, though, that Intel does publish addendums to the JEDEC DDR specifications?

A. I'm not aware, but I have no knowledge one way or another.

Q. You're not aware of the fact that Intel has published an addendum for the DDR DIMM specification?

A. I have never -- I'm not aware that they -- they may do a lot of things with their partners that I am just not aware of all the stuff, communication they have with their partners.

Q. When you were designing the chipset for the AMD 760 that was compatible with DDR --

A. Correct.

Q. -- didn't you have to look at some of Intel's addendums on the DDR 200 specification, for example?

A. No. Intel wasn't participating to our knowledge at that point.

Q. So you're not aware of whether or not they have addendums to the DDR specifications?

A. No.

Q. Didn't they write the PC100 standard?

A. I have no knowledge. I didn't think so, but I have no knowledge one way or another.

Q. Okay. Why don't I show you -- let's bring up RX-2103-14.

May I approach, Your Honor?

JUDGE McGUIRE: Yes.

BY MR. GATES:

Q. Okay. Mr. Polzin, do you recognize that as the Intel PC SDRAM standard?

A. That's what it says on the front, yes, sir.

Q. And did you use that standard when you were designing the AMD 750 chipset?

A. Probably among others we used this, yeah, among other specifications this is probably one we looked at, yeah.

Q. So when you were designing the AMD 750 chipset,

you were looking at the Intel standard?

A. Among others, yes.

Q. You also talked earlier about your efforts with the -- to develop the Rambus controller. Do you remember that?

A. Yes.

Q. Okay. And you had looked at a document where you laid out kind of the chronology of your efforts?

A. Yes.

Q. Okay. Let's look at that, CX-2158. Do you have that?

A. Yep.

Q. Okay. Now, if you look down at something Mr. Davis pointed to where it says, on the first page, Rambus offered to complete -- offered a complete system picture?

A. Uh-huh.

Q. And you explained to us that Rambus had already specified a number of items in the infrastructure; right?

A. Yes.

Q. And it was important to you at the time because the DDR specification hadn't been settled upon; right?

A. Yes.

Q. And the DDR infrastructure had not been specified?

A. Yes.

Q. But the Rambus infrastructure at least had been specified at this point; right?

A. Yes.

Q. And I think you referred to something -- you referred to a term, you said it's important that the specifications be vendor neutral; right?

A. Correct.

Q. Were the Rambus -- those Rambus specifications were vendor neutral, weren't they?

A. Yes.

Q. Okay. And you also said that, well, you might have a DRAM, but just having a DRAM is not enough, you have to have all this infrastructure; right?

A. Yes.

Q. So without the system infrastructure, you can't have a memory system even if you have that DRAM?

A. Correct.

Q. Okay. And the reverse is true as well; right? If you don't have the DRAM, all that infrastructure is useless; is that right?

A. Yeah.

Q. So if the DRAM manufacturers aren't going to

be producing a particular type of DRAM, no matter what you do with all the infrastructure, it's not going to work?

A. Correct.

Q. And at the time when you were designing this chipset for the Rambus RDRAM, it was later on when you'd made the decision to switch to DDR, it was your understanding that RDRAM was not going to become the commodity product; right?

A. No. Our understanding was it was -- the reason that we shelved it -- we were very careful to make sure we could restart the project -- it was a timing thing. It was clear it wasn't going to be a commodity product in the time frame of interest.

Q. So it was your understanding at least that the reason why you switched over and put all your efforts into a DDR controller was because DDR was going to be the volume product?

A. Yes.

Q. And you understood that from what you were hearing from the memory manufacturers?

A. Yes.

Q. At the very bottom of that page, of that e-mail, the first page, you refer to future K8 implementations became clear with respect to

difficulties of getting the Rambus controller on the die; right?

A. Yes.

Q. And that you were talking about putting the memory controller actually on the CPU or on the same die as the CPU?

A. Yes.

Q. And you're referring -- I guess you said earlier that there were some difficulties in doing that with the K8?

A. Yes.

Q. Now, you're familiar with the Alpha processor; right?

A. The old ones.

Q. Okay. When you were at DEC, you worked on the Alpha processors?

A. Correct. Yes.

Q. And DEC later changed and finally became part of Compaq; is that right?

A. That's correct, yes.

Q. And Compaq is using the Alpha processors in their high-end servers; right?

A. Yes.

Q. And are you aware of the fact that the Alpha processors have incorporated the Rambus controller onto

the die with the CPU?

A. I wasn't aware of that, but it sounds reasonable.

Q. Why does it sound reasonable to you?

A. I know that was their direction they told us in, jeez, I don't know, 1996 or '97.

Q. So you knew in 1996 or 1997 that DEC or Compaq, whichever it was at the time, was planning to incorporate the controllers on the die?

A. Yes.

Q. And you knew they were trying to do that with the RDRAM?

A. Yes.

Q. You just weren't sure whether or not they finally did that?

A. Yeah, I just wasn't sure, yeah.

Q. And did you know that Intel has done this same thing with some of their network processors?

A. No. I wasn't aware.

Q. Did you know that Sony has done that with a Playstation 2 processor?

A. No. I wasn't aware.

Q. So it's not impossible to put the Rambus controller onto the die in the K8; right?

A. Doing it once is not the problem; it's keeping

it -- keeping that processor competitive as you constantly tweak the process to get faster and faster processors, which you require in the desktop microprocessor marketplace.

Q. Do you consider the Alpha processor competitive?

A. No.

Q. No. Okay. So just because Compaq uses it in its high-end servers it's not competitive?

A. It's not very competitive anymore in the marketplace. That's why it's dying.

Q. At one time it was; right?

A. At one time it was, yes, sir.

Q. And do you consider Intel's network processors to be competitive?

A. I'm not very aware of how the network processor space, you know, stacks up, so I don't have any knowledge of that.

Q. Further down on that second page of the e-mail we're looking at you get some dates.

And you started the process of developing a DDR controller in early '99; is that right?

A. That's correct, yes.

Q. And then in April of 1999 you put your Rambus efforts on the shelf?

A. Correct.

Q. Then by December of 1999 it says AMD powered up the first K7 DDR chipset?

A. Yes.

Q. So within three-quarters of a year or so you were able to develop that chipset?

A. Yes.

Q. And it also talks about IGD4-based motherboards, you had samples in March of 2000?

A. Yes.

Q. Prior to your efforts in early 1999, were any motherboard manufacturers developing motherboards to be compatible with AMD processors and DDR memory?

A. Not that I'm aware of.

Q. So they were able to in some about less than a year maybe develop those motherboards?

A. In what time frame are you referring to the year?

Q. Well, they had samples coming out in March 2000; right?

A. Correct.

Q. And you started this whole effort in early 1999; right?

A. Correct.

Q. So they were working in parallel?

A. The motherboard companies?

Q. The motherboard companies.

A. No. The motherboard companies -- we enabled the motherboard companies at about the same time in March of 2000 for our chipset.

Q. So you enabled the motherboard companies in March 2000 and so it was your samples --

A. Yes.

Q. -- motherboard samples?

Okay. So by September of 2000 the motherboard manufacturers were able to mass-produce motherboards compatible with the IGD4 chipset?

A. Yes.

Q. We talked about earlier something -- the VLSI rump session. Do you recall that?

A. Yes.

Q. Where you gave a presentation?

A. Yes.

Q. And when you gave that presentation, it was your understanding that each of the participants had a different role; right?

A. Yeah. Yeah.

Q. So you were the DDR guy --

A. Correct.

Q. -- right?

And you were there to advocate the DDR position; right?

A. Yes.

Q. And at that time AMD had decided to go with DDR?

A. Oh, yes. Yes. Yes. We had been in production I believe at the time.

Q. And so you were there to present all the positive aspects of DDR; right?

A. Yes.

Q. And you weren't intending to present any of the negative aspects, if there were any, of DDR?

A. No, I was not intending to present any negative aspects of DDR.

Q. And there were other people there who were advocating other memory technology; right?

A. That's correct.

Q. There was someone there advocating SDRAM?

A. Yes.

Q. And there was someone there advocating RDRAM?

A. Yes.

Q. Was that Mr. Kim from Samsung?

A. No.

Q. Who was advocating RDRAM?

A. It was a gentleman from Intel. His first name

was John; I don't remember his last name.

Q. But there was somebody from Samsung there participating; right?

A. Yes.

Q. And do you recall the person from Samsung was very pro Rambus?

A. I don't recall.

Q. His name was Dr. Kim? Do you remember that?

A. I believe it was Dr. Kim, but I don't recall what he was advocating, what position he was advocating.

Q. Well, you say in your presentation -- you said one of the problems with RDRAM was testing costs; right?

A. Yes.

Q. Okay. And you had heard that from some of the memory manufacturers; right?

A. That's correct.

Q. And when you were doing this presentation, you were taking the, quote, total DDR position; right?

A. Correct.

Q. And by "total DDR position" you meant you were not talking about only the chipset side of things, you were talking about the whole infrastructure?

A. I was attempting to, yes.

Q. And so in order to put forth the total DDR position, you were trying to spit back some of the things that the DRAM manufacturers had told you about DDR?

A. Yes.

Q. So some of the things that are in your presentation at least were just coming directly to you from the DRAM manufacturers; right?

A. Yes.

Q. And you didn't go out to the DRAM manufacturers to verify everything they were telling you, did you?

A. No.

Q. So you were just putting forward what they were telling you in your presentation?

A. Yes.

Q. And if you look at the first page of your presentation -- I guess that was RX-1839, page 7 -- in the first page of your presentation your number one point, the first point that you made was about pricing; is that right?

A. Yes.

Q. And your point there was that the price of DDR had dropped tremendously because there was volume of DDR shipping; right?

A. Yes.

Q. And you also -- your second point was that it was available. That means there were -- the DRAM manufacturers were making it; right?

A. Yes.

Q. And that was in contrast to RDRAM, for example? RDRAM had less availability?

A. I didn't make any specific statements to that effect, but the intent was to show that this was available.

Q. You were trying to advocate the kind of advantages of DDR over other types of memory; right?

A. Yes.

Q. And one of the advantages was that it was available while others were not?

A. Yes.

Q. And Mr. Davis asked you about some different alternatives for Rambus technologies.

A. Yes.

Q. And the first time you thought of any of these alternatives was in 2000; right?

A. Yes.

Q. And let me just understand some of your background.

Had you ever designed a DRAM chip before?

A. No.

Q. You've designed microprocessors, but those are different from DRAMs; right?

A. Yes.

Q. And are you familiar with DRAM manufacturing processes?

A. No.

Q. Are you familiar with DRAM manufacturing costs?

A. No.

Q. And so when you told us that some of the alternatives that you had thought of wouldn't have an impact on costs, did you know whether or not it would have an impact on the manufacturing costs of the DRAM?

A. I had some discussions with a few DRAM partners, and that's where that data came from. That's where my opinion came from on that matter.

Q. Now, let me ask, when you at AMD are confronted with a new DRAM design, something that's been changed, do you just take the manufacturer's word that the change is going to work?

A. So it depends on what you mean by "change," so if it's a minor spec change or a minor manufacturing change, we will do a retest to make sure everything is fine.

Q. Okay.

A. If that's what you're referring to.

Q. Let's take a change on the magnitude of some of the things you suggested where you would -- might change a function so that instead of doing it in a register, you're doing it through pins.

A. Uh-huh.

Q. If a manufacturer came to you and said, well, we're going to do it differently now, you would want to see some kind of simulation to make sure that works; is that right?

A. Well, there were -- yeah. Yes. We would want to see some sort of verification that it worked.

Q. And if you don't have an actual part, you might simulate it on a computer; right?

A. Yes.

Q. And if you do have an actual part, you would test that; right?

A. Assuming you had a memory controller that interfaced to it, yes.

Q. Okay. So if you had a memory controller that interfaced to it, you would test it to make sure it works; right?

A. Yes.

Q. Did you do any kind of simulations for any of

the alternatives that you suggested today?

A. No.

Q. Did you do any kind of testing for any of the alternatives that you suggested to us today?

A. No.

Q. Did you do any analysis to determine whether or not the alternatives that you suggested today would be covered by Rambus' patents or any other person's patents?

A. Well, the intent was to make sure it was not covered by the Rambus patents, that the work-around avoided the Rambus patents. That was the objective. So I don't quite understand your question I guess.

Q. Okay. Let me back up.

Did you do any analysis to verify whether or not the alternatives you came up with were patented or not?

A. No.

Q. So you don't know whether or not there's a patent out there that covered some of the alternatives that you suggested?

A. Correct.

Q. One of the alternatives that you talked about was pin strapping; right?

A. Yes.

Q. And the way to implement that would be to actually add pins to the DRAM and use those, post those?

A. That's one way of doing it, yes.

Q. And if there were no available pins on the DRAM, you'd have to add pins to the package; right?

A. Or multiplex existing pins.

Q. Well, one way to do it would be to add dedicated pins?

A. One way to do it.

Q. And if there are no connected pins, then you're going to have to add pins to the package?

A. You don't necessarily have to. You could use existing pins and multiplex them.

Q. And I'm asking you in the situation where you're not multiplexing them.

A. Yes. You would have to add them in, yes.

Q. For CAS latency, how many values are specified by the JEDEC DRAM/SDRAM standard?

A. Oh, boy.

Q. Is it three?

A. It's either one, two or three. It's -- it's either one or two bits, which is up to four states.

Q. So --

A. I don't know for certain. I don't have the

spec memorized.

Q. If it's two bits, then you would need two?

A. Two pins, that's correct.

Q. Two pins. Okay.

Let me call up RX-2100-13.

Your Honor, may I approach?

JUDGE McGUIRE: Yes.

BY MR. GATES:

Q. Now, Mr. Polzin, you've seen DRAM spec sheets like this before; right?

A. Yes.

Q. And you are familiar with pinout diagrams like the one that's depicted on the first page; right?

A. Yep.

Q. So you would be able to read that particular pinout diagram?

A. Yes.

Q. At the x16 density -- is that the right word, the "by 16"?

A. Yes.

Q. At the x16 density can you tell me how many no-connect pins are in this particular type of DRAM?

MR. DAVIS: Objection, Your Honor. It calls for expert opinion.

JUDGE McGUIRE: Mr. Gates, response?

MR. GATES: Your Honor, he's just told us that he's familiar with these types of data sheets, that he's familiar with these types of diagrams and that he would be able to read the pinout diagram that's there on the page.

JUDGE McGUIRE: Overruled. If he can answer that, I mean, he's gone through quite a bit here, so if he can answer the question, he can go ahead.

MR. GATES: Thank you, Your Honor.

THE WITNESS: The question is how many no-connect pins are available on the x16 version of this part. And I believe the answer is one. If I can read this properly.

BY MR. GATES:

Q. So under the alternative that we were just discussing, in order to implement that alternative on this particular DRAM, you would have to add a pin; right?

A. Yes.

Q. Now, you also talked about a multiplexing option.

So we understand that, you would send data over at reset that would specify the CAS latency; right?

A. Not necessarily send. Pins could be allocated

at reset to be again pulled up to a high voltage or pulled down to a low voltage through a high value resistor so that they wouldn't affect normal operation, but that value could still be read by some internal logic at reset time, as you suggested.

Q. And so that information about what the CAS latency is would be received by the DRAM at reset?

A. Correct.

Q. And in order for that to operate, that information would have to be stored somewhere in the DRAM; is that right?

A. Correct.

Q. And you would store that in the register?

A. Correct.

Q. You also talked about various options, alternatives for programmable burst length; right?

A. Yes.

Q. And one of the options that you talked about was pin strapping again; right?

A. Yeah.

Q. And in order to implement that without multiplexing you would have to have a dedicated pin, at least one?

A. Yes.

Q. So if you wanted to have two burst length

options you'd have to have one pin; is that right?

A. Correct.

Q. If you wanted to have three burst length options you'd have to have two pins; is that right?

A. Yes.

Q. So if you implemented that alternative with -- the pin strapping alternative that we discussed with CAS latency, you would have to add two or three pins; right?

A. I think you're combining both work-arounds together.

Q. I am.

A. And yes, so you would have to add pins or use more multiplexed pins as you added more features.

Q. And not only would you have to add pins on the DRAM, but you might have to add pins on the DIMM as well if there were not one -- DIMM pins available; is that right?

A. That -- in one case, yes.

Q. And then you'd have to have pins at either the memory controller or some other controller; is that right?

A. Yes.

Q. And pins add cost?

A. Yes.

Q. The more pins, the more cost?
A. Correct.
Q. I think you talked earlier about when you were at Apple -- well, I'm sorry. Let me back up. I've missed something on programmable burst length. I apologize.
You also talked about multiplexing with -- in order to program the burst length; right?
A. Yes.
Q. And the same as we discussed with CAS latency, the DRAM would receive that information at reset?
A. Yes.
Q. And that information would have to be stored in the DRAM as to what the burst length is; right?
A. Yes.
Q. And that would have to be stored in a register?
A. Sure. Yes.
Q. I'm sorry. Now we'll go to Apple.
You discussed earlier with Mr. Davis when you were at Apple that Apple was using EDO technology; right?
A. I believe so, yes.
Q. And EDO is an asynchronous technology?
A. That's correct.

Q. SDRAM is a synchronous technology?

A. That's correct.

Q. And your opinion back in the 1996-97 time frame when you were looking at the two technologies was that synchronous had more headroom than asynchronous; right?

A. If you're referring to Apple, I was not at Apple in '96 and '97.

Q. I apologize. Let's look at the time frame.

In 1996-97, you're right, you were at AMD at that time; right?

A. Yes, sir.

Q. And your opinion was in that time frame that synchronous technology had more headroom than asynchronous technology?

MR. DAVIS: Objection. Calls for expert opinion.

JUDGE McGUIRE: You know, I'm a little -- it's getting to where, I mean, I think he's obviously an expert and for him to determine what's he's testifying to from his personal knowledge is a pretty fine line here, so it's hard for the court to determine whether he's testifying now as an expert or not.

MR. GATES: Your Honor, I'm asking for what his opinion was when he was looking at the technology.

JUDGE McGUIRE: I'll entertain the question on that basis.

MR. GATES: Thank you, Your Honor.

BY MR. GATES:

Q. Do you have the question in mind?

A. No. Could you please --

Q. Let me back up and then I'll ask the question because I used a term that maybe not everyone is familiar with.

You're familiar with the term "headroom"; right?

A. Yes.

Q. And what does that term mean to you?

A. That there is growth in some parameter, frequency, performance, capacity, using a similar technology as you go over time, that you don't have to radically change something to go to the next increment of performance or capacity or frequency.

Q. And you've used the term "headroom" with respect to DRAM technologies; right?

A. Probably. I don't think this morning or today I did, but yes, I've probably used it in my career at some point, yes.

Q. Okay. And to go back to my question that we were discussing earlier, going back to the

1996-1997 time frame, wasn't it your opinion in that time frame that synchronous technology had more headroom than asynchronous technology?

A. Yes.

Q. And why was that?

A. The -- well, the industry was pushing that way to start with. DRAM manufacturers were telling us that's where they were going. They were obsoleting their synchronous technology. In other areas of computer systems, not necessarily DRAMs, but other areas, synchronous technology had overtaken long ago. Semi clocks with data was an established way for many, many years and getting DRAMs onto that technology was clearly the right thing to do.

Q. Is there anything inherent about asynchronous technology that makes it have less headroom than synchronous technology?

A. The most obvious thing would be the fact that most asynchronous data transfer technology requires timing to be defined by delay lines or delay parameters, and those things -- delay lines or delay parameters constructed out of semiconductor devices will vary as the process, voltage and temperature of the device changes over time. As your cycle time becomes smaller and smaller, your frequency higher and

higher, those sorts of things will dominate and cause errors.

Q. Now, you're also familiar, aren't you, with a technology developed by Kentron called QBM?

A. Top-level familiarity, yes.

Q. You've seen presentations?

A. Yes, I've seen presentations from Kentron.

Q. Did you do a preliminary evaluation of that technology?

A. Very preliminary. Basically I saw their presentation.

Q. Okay. And you understood that their technology is basically interleaving banks on a DIMM, interleaving memory banks on a DIMM?

A. Yes.

Q. And they use a FET switch, F-E-T switch, to do that?

A. Yes. That's my understanding.

Q. And your preliminary evaluation of that technology was that it would have signal integrity problems?

A. Yes.

Q. Can you explain to me why you came to that conclusion?

A. My first exposure to the Kentron stuff was in

the context of using signal data rate DRAMs using the FET switch that you described to multiplex two devices at twice the data rate on one wire. And our immediate concern was that trying to use the signaling technology or I/O specification of the synchronous data -- synchronous DRAM to drive twice as fast wouldn't work very well. Given that it was having problems working very well at its low speed, doubling it didn't seem to be the right thing to do.

Q. You're familiar with a term called a burst terminate command?

A. Yes.

Q. Can you explain what that is, what is a burst terminate command?

A. This is a command used in synchronous DRAM technologies, including DDR, where a burst command is a command that says I want to do an operation with a long sequence of data, four or eight cycles worth of data, and the burst terminate command is I believe used after a burst command has started to stop that command before it completes.

Q. And is another name for that a burst interrupt command?

A. I believe so, yes.

Q. And so, for example, when we're talking about

programmable burst length, that's a burst of data, is that the same type of data that -- burst of data that we're talking about with the burst terminate command?

A. Yes.

Q. Let me show you a document that's RX-1388.

May I approach, Your Honor?

JUDGE McGUIRE: You may.

BY MR. GATES:

Q. Mr. Polzin, I've handed you a document that is an e-mail from Jim Keller to you?

A. Yep.

Q. Attaching something from a future DRAM task force. Do you see that?

A. Okay.

Q. Okay. I just want to ask you about something on a particular page, and that is page 6.

If you look down near the bottom of the page, there is a bolded text that says "No read or write burst interrupt commands."

Do you see that?

A. Yes.

Q. And then it says -- I think it should be "at," but it says, "A high data rates burst interrupt commands are of less value and are more difficult to engineer."

Do you see that?

A. Yes.

Q. Okay. Do you agree with that statement, based on your experience?

A. Yeah, this is referring to the details of a DRAM design of which I'm not expert in. But it sounds plausible to me.

Q. Well, let me ask you it this way.

Isn't your understanding that the use of a burst interrupt command can waste command bandwidth?

A. It could be used in a manner that would waste bandwidth, yes.

Q. And isn't it your understanding that the use of a burst terminate command can lead to a less efficient system overall?

A. Yes.

Q. And why is that?

A. The -- my understanding of the issue is that to use the burst terminate command you cannot start an operation until all of the data has been received in case there was a terminate command halfway in between. You have to wait for the entire thing to happen to make sure no terminate commands happened while you were receiving the data and then actually perform the operation inside the chip.

Q. Have you heard of the term "pipelining"?
A. Yes.
Q. And are you familiar with what that term means?
A. Yes.
Q. What is your understanding of pipelining?
A. Pipelining means that small parts of -- let me back up.

Pipelining is that an operation can be broken into small parts and executed on a series of data in successive stages, so in cycle one the first data will get operated on the first part of the operation, cycle two the second, but immediately following the next data can be working on the first operation.

It's better if I could draw it if you really want me to, but --
Q. Just a high-level explanation is fine.
A. Yes.
Q. If I understand the concept, pipelining is used to increase the efficiency of microprocessors?
A. Yes.
Q. And for synchronous DRAMs, those are pipelined; is that right?
A. Yes.
Q. And is it your understanding that the use of a

burst terminate command can mess up your pipelining?

A. Yes.

Q. You were talking about earlier with Mr. Davis about some alternatives for dual-edge clocking. Do you remember that?

A. Yes.

Q. And you were concerned when you were looking at these alternatives in 2000 that to implement them it would mess up things because you were in the middle of a product launch; right?

A. Yes.

Q. Okay. And that was in the middle of the product launch for DDR; right?

A. Correct.

Q. And you had been designing things for DDR in 1999 prior to 2000; right?

A. Yes.

Q. And so in fact the decision to go to DDR was sometime in early 1999?

A. Correct.

Q. So if you had known prior to that time that Rambus' patents would be infringed by the use of dual-edged clocking and one of your alternatives were adopted in the JEDEC standard, would you have had those same concerns?

MR. DAVIS: Objection. Calls for speculation.

JUDGE McGUIRE: Sustained.

BY MR. GATES:

Q. You were concerned because you were in the middle of a product launch; right?

A. I was concerned about what?

Q. You were concerned about implementing these alternatives because you were in the middle of a product launch?

A. Correct. Yes.

Q. Would you have had those same concerns if you weren't in the middle of a product launch?

MR. DAVIS: Objection. It's the same question.

JUDGE McGUIRE: Sustained.

MR. GATES: Thank you, Your Honor.

BY MR. GATES:

Q. What was it about the fact that you were in the middle of a product launch that raised these concerns?

A. We had enabled a number of DRAM manufacturers, motherboard manufacturers, our own manufacturing of our chipset assuming one standard, one spec. To change that, we'd have to stop all that production, reengineer, redeploy, start production again. It

would be detriment -- seriously detrimental to our business.

Q. And when you decided to go to DDR instead of Rambus, did you have to reenable your vendors and redesign your chipset at that point?

A. We, based on -- well, from what basis?

Q. Well, in early 1999, you decided that instead of going with Rambus to go with DDR; right?

A. Yes.

Q. Okay. And I'm wondering whether or not you had to go through the same types of things that you were concerned about when you looked at the Rambus patents in 2000 in the middle of a product launch.

A. Well, given that we were starting essentially from, you know, a certain base and starting forward, you know, we could have done pretty much anything, if you want to call it that.

Q. So if I understand what you're saying, if you're starting at a zero base you can implement these alternatives?

A. Yes.

Q. Costlessly?

A. Yes.

Q. So for example, you're working on chipsets for -- you worked on chipsets for DDR-II; right?

A. No.

Q. You worked on a processor that's going to be compatible with DDR-II?

A. Personally, no, I'm not working on that, that product.

Q. You're not working on the K8?

A. No. I'm the system guy. I'm not the microprocessor guy. I'm sorry. I'm not following your question here.

Q. So you're the system guy?

A. Yes.

Q. For K8?

A. Yes.

Q. So your job is to make sure that there's an infrastructure for the K8?

A. Correct. Yes.

Q. And you based your determination of using DDR-II on what you knew was going to be or what you thought was going to be available in the marketplace; right?

A. So DDR-II is a future technology. We don't have any products out for DDR-II. I'm --

Q. You're developing products for DDR-II; right?

A. Yes.

Q. And you're developing -- you're working on

developing an infrastructure for DDR-II; right?

A. We're starting, yes.

Q. When did that start?

A. It technically hasn't started. We haven't really started that yet.

Q. It hasn't started?

A. Yeah.

Q. So if the DDR-II specification were to adopt some of your alternatives, that would be starting at ground zero as far as AMD is concerned?

JUDGE McGUIRE: All right, Mr. Gates. I'm not sure where you're going at this point. I'm not sure you're still within the scope and I'm going to ask you to change your line.

MR. GATES: Okay. Thank you, Your Honor.

BY MR. GATES:

Q. You said earlier that you had discussions with some DRAM manufacturers about the alternatives that you had come up with?

A. Yes.

Q. And those discussions happened in 2000; is that right?

A. Yes.

Q. And you're aware of the DDR-II specification; right?

A. I believe it was winding its way through JEDEC at the time, yes.

Q. So the DDR-II specification at the time in 2000 was winding its way through the -- through JEDEC; right?

A. Yes.

Q. Okay. The DDR-II specification uses programmable CAS latency; right?

A. That's my understanding, yes.

Q. And it uses --

MR. DAVIS: Objection, Your Honor. This is beyond the scope. We didn't talk about DDR-II at all in direct.

JUDGE McGUIRE: Sustained.

MR. GATES: Your Honor, I'd like a little leeway here only because I don't want to have to call this witness back on direct in our case. I have one small line of questioning on DDR-II and that will be it. I thought that was our understanding with complaint counsel, but I'm apparently wrong.

JUDGE McGUIRE: Then, Mr. Davis, did you have any sort of agreement with respondent on that?

MR. DAVIS: No objection, Your Honor.

JUDGE McGUIRE: All right. Go ahead, Mr. Gates.

MR. GATES: All right. Thank you, Your Honor.

BY MR. GATES:

Q. Okay. So it's your understanding that the DDR-II specification specifies programmable CAS latency; right?

A. Yes.

Q. And it specifies using a mode register to set the CAS latency?

A. I believe so, yes.

Q. And the DDR-II specification is not completed yet; right?

A. The JEDEC specification is pretty darn close to completion, but yeah, I guess it's never quite at the end.

Q. And it's now 2003, it's not quite at the end; right?

A. Yeah. Yeah.

Q. And the DDR-II specification specifies programmable burst length; is that right?

A. I believe so.

Q. And were you aware of the fact that at one point it was considered to just use a burst length of four in the specification?

A. I'm not aware of that. But I have no knowledge one way or another.

Q. You know now, though, that it specifies programmable burst length?

A. Yes.

Q. And it specifies using a mode register?

A. Yes.

Q. And that's the same way it's done in DDR?

A. Yes.

Q. And going back to programmable CAS latency, it specifies the same way programmable CAS latency is done in DDR; is that right?

A. Yes.

Q. And DDR-II uses dual-edged clocking; right?

A. Yes.

Q. And it's basically the same technology that was used in DDR; right?

A. Yes.

Q. And when you reviewed the Rambus patents in 2000, you understood that they covered programmable CAS latency in DDR?

A. Yes.

Q. And you understood that they covered programmable CAS -- programmable burst length in DDR?

A. Yes.

Q. And you understood that they covered dual-edged clocking in DDR?

A. Yes.

MR. GATES: No further questions, Your Honor.

JUDGE McGUIRE: All right. Thank you, Mr. Gates.

Mr. Davis?

You may want to mark this sheet as DX-31, Mr. Gates, if you would.

MR. GATES: Thank you, Your Honor.

(DX Exhibit Number 31 was marked for identification.)

JUDGE McGUIRE: All right. Mr. Davis?

MR. DAVIS: Thank you, Your Honor.

JUDGE McGUIRE: Redirect.

REDIRECT EXAMINATION

BY MR. DAVIS:

Q. Mr. Polzin, would you describe what "front-side bus" means on that (indicating).

A. "Front-side bus" is an industry term that refers to the main interface from the microprocessor to the Northbridge chipset. It's typically a wide bus, primarily used for transfer of memory data.

Q. Now, were you involved in the project that moved the front-side bus for AMD from 200 megahertz to 266 megahertz?

A. Yes.

Q. Were you involved in the decision to do that?
A. Yes.
Q. Why was AMD moving from 200 megahertz to 266 megahertz on the front-side bus?
A. To increase performance of the system.
Q. Why was that important?
A. To remain competitive in the marketplace.
Q. And why were you moving -- were you involved in the decision to move from 266 megahertz to 333 megahertz?
A. Yes.
Q. And do you know why that was done?
A. Similar reasons, always to get more and more performance for our customers.
Q. And so it's the same reason -- were you involved in the decision to move from the 333 to the 400?
A. Yes.
Q. Was that also the same --
A. Same, same reason.
Q. Did that improvement in performance from the 200 to 266 and the 266 to 333 and the 333 to 400, did that have any implication for your chipset or motherboard suppliers and partners?
A. Yes. Our chipset partners needed to design

faster circuitry in their chipsets and our motherboard partners needed to adhere to stricter design rules in their manufacture of their motherboards.

Q. Was there any benefit to the chipset manufacturers or the motherboard manufacturers if they did design to the higher speeds?

MR. GATES: Object, Your Honor, on foundation grounds.

JUDGE McGUIRE: Sustained.

BY MR. DAVIS:

Q. Do you have any understanding of why your chipset partners manufactured your chipsets for your front-side buses?

A. Why they manufacture our chipsets for the faster front-side buses? That's the question? They want to keep up with the latest technology. They can get higher prices for more advanced chipsets. A chipset that supports DDR 333, for example, is worth more than a chipset that supports DDR 200.

Q. What's your basis for saying that?

A. Well, when we were in -- when AMD was in the chipset business and selling our DDR chipset, our DDR chipset we could sell for more money than our single data rate chipset. And we closely track our third-party chipset prices and motherboard prices as

part of our ongoing business to make sure our microprocessors match up in the right marketplace.

Q. Now, do you have an understanding then of why -- of the benefit to the chipset manufacturers and the motherboard manufacturers of increasing -- of working with the increased front-side bus?

A. Yes. The benefit is they can then use faster -- better-performing microprocessors and deliver a better-performing system to customers and therefore be able to keep up with the competition and retain their prices, retain their market share in the given price points that they want to participate.

Q. Thank you.

Now, earlier you were discussing synchronous DRAM with Mr. Gates. Do you remember that?

A. Yes.

Q. And the difference between synchronous DRAM and asynchronous DRAM?

A. Yes.

Q. When you were referring to the term "synchronous DRAM," were you -- sorry.

When you were referring to the term "asynchronous DRAM," did that include the DRAM where there was a data strobe or some other strobe?

A. No. Asynchronous DRAM -- I'll just use the

industry terms. Asynchronous DRAM I refer to as the fast page mode and the EDO versions of DRAMs. Synchronous DRAM -- synchronous technology started in my mind with SDRAMs.

Q. So when you were talking about synchronous DRAM and asynchronous DRAM, a DRAM that was asynchronous except that it had a data strobe, that would come under your definition of synchronous or asynchronous?

A. I believe that that would have to fall under asynchronous. My definition is synchronous starts out with the synchronous DRAM specs. The PC66, the PC100, that's the start of synchronous technology in my -- in what I was referring to.

Q. Okay. When you were referring to Kentron and the signal integrity problems that you observed when you saw that presentation --

A. Yes.

Q. -- what was the cause of those signal integrity problems?

A. The basic cause is that they were trying to use a driver technology that was designed to run at a hundred megahertz speeds, for example, using PC100 DRAM parts and run that twice as fast using the same I/O signaling technology.

Q. Did you have any understanding at the time whether that I/O signaling technology could have been improved so that this Kentron solution could work?

MR. GATES: Objection, Your Honor. It lacks foundation and it calls for opinion.

JUDGE McGUIRE: It calls for opinion?

MR. DAVIS: This is exactly the topic that he was referring to earlier.

MR. GATES: Well, you're --

JUDGE McGUIRE: Well, I'm going to -- that's overruled. I'll let him, to the extent he had an understanding at the time, I'll let him answer.

THE WITNESS: I'm sorry. Could you repeat the question.

BY MR. DAVIS:

Q. Yes.

Did you have an understanding at the time of whether an improved signaling technology would have allowed the Kentron system to work whereas the signaling technology then on SDRAMs wouldn't allow it to work?

A. I believe in the time frame that we were discussing, this particular Kentron technology, they probably could have invented a new signaling technology, certainly the one used for DDR, for

example, but it would have required a brand-new DRAM, manufactured DRAM I/O cell design, and I don't believe that's the basis of their technology.

The basis of their technology from my understanding is they use, quote, old DRAMs and you run them twice as fast through your magic FET switches, and it just doesn't work that way.

MR. DAVIS: Okay. Thank you, Your Honor.

JUDGE McGUIRE: Mr. Gates, any recross?

MR. GATES: No, Your Honor.

JUDGE McGUIRE: All right, sir. Thank you very much for your testimony today. You're excused from these proceedings.

Let me ask from I guess complaint counsel, what's on tap for Tuesday? I know we talked the other day that that was still somewhat up in the air. Maybe we can get an update.

MR. OLIVER: Yes. Excuse me. We had had a scheduling problem tomorrow. We don't have a witness for tomorrow. We're hoping to be able to read in some depositions, and I think, based on what you said at the beginning of this afternoon's session, I think the question I have for you is, after you issue your order tomorrow, would we then be in a position to play and read in Dr. Oh's testimony?

JUDGE McGUIRE: Yes, you would.

MR. OLIVER: Then I think I guess I would suggest if we could await your order and then do that tomorrow.

JUDGE McGUIRE: Okay. You mean -- I'll plan on having it out in the morning. Do you want to postpone then the hearing for an hour or so after I issue the order? What are you suggesting that we do?

MR. OLIVER: I think that would work very well for our side.

(Pause in the proceedings.)

We were discussing perhaps starting at 11:00 in the morning.

JUDGE McGUIRE: That's fine. That's fine. We'll start at that time then.

Anything else?

MR. GATES: No, Your Honor. I just had one exhibit that I needed to move in.

JUDGE McGUIRE: Go ahead, Mr. Gates.

MR. GATES: I'd like to move in RX-2100-13. That's the spec sheet.

JUDGE McGUIRE: Any objection?

MR. DAVIS: No objection, Your Honor.

JUDGE McGUIRE: So entered.

(RX Exhibit Number 2100-13 was admitted into

evidence.)

JUDGE McGUIRE: Okay. Very good. We'll convene tomorrow morning.

And Mr. Stone, I'm hopeful you'll keep us informed on the pending birth of your colleague's child immediately.

MR. STONE: I certainly will, Your Honor. Thank you for inquiring.

JUDGE McGUIRE: Thank you very much. Hearing in recess.

(Time noted: 3:44 p.m.)

C E R T I F I C A T I O N O F R E P O R T E R

DOCKET NUMBER: 9302

CASE TITLE: RAMBUS, INC.

DATE: June 2, 2003

I HEREBY CERTIFY that the transcript contained herein is a full and accurate transcript of the notes taken by me at the hearing on the above cause before the FEDERAL TRADE COMMISSION to the best of my knowledge and belief.

DATED: June 2, 2003

JOSETT F. HALL, RMR-CRR

C E R T I F I C A T I O N O F P R O O F R E A D E R

I HEREBY CERTIFY that I proofread the transcript for accuracy in spelling, hyphenation, punctuation and format.

DIANE QUADE