- DRAM users
- JEDEC participants
- DRAM plant managers
- DRAM engineers

Interviews Conducted
Case Study

Standards

Choices among alternative DRAM technologies

Purpose: Assessing economic factors influencing trade press, analyst reports, discovery materials

Information sources: publically available materials

Time period: 1990 to present

Focus: Evolution of DRAM standards / technologies

Private reports and information

Methodology: Comprehensive review of public /
DRAM Chip Manufacturers in the Past
Economics of DRAM Production

- Intense cost cutting
- Maximize capacity utilization / yield
- Intense price competition
- Volatility / cyclical
- High fixed costs
Total Cost and Fixed Cost
Larger water size
Die shrinks
Optimized production process
Extended equipment life
Clean rooms
24/7 operation

Costs / Increasing Yields
Reducing DRAM Production
Evoluutionary / Revolutionary

Manufacturing costs

Implementation costs

Royalties

Open availability of standard

Open, consensus-based process

DRAM Standards

Economic Factors Influencing Success of
Valid technical justification

members

RAND: mandatory for JEDC; voluntary for

applications relevant to JEDC standards / work

Disclosure applies to patients / patient

Early disclosure / good faith

Preference to avoid patients

JEDC: IP Disclosure
Macrion Trial Testimony at 4763-64

- Potentially higher inventory costs to DRAM manufacturers
- and burst length. "Macrion Trial Testimony at 4773
- every function in the DRAM, including programmable CAS
- point of view; there would have been an advantage to fixing
- feature to the DRAM, you have to test it. So, from a test cost
- "A fixed DRAM is easier to test. Every time you add a new
- Cost Impact

- NEC presentation at 42.3 Committee Meeting 76 (9/95)
  - Presented at JDEC
  - Fixed CAS Latency

Latency Technology Market
products on, being smart. "Macro Trial Testimony at 4767
minimal, and that's what you know, we try to build the
you're smart, you do it in a way where the cost is exceeding
have been to add extra pins on the DRAM? A. Yes, but it
C. So, one of the costs of these -- of this alternative would
Cost Impact

(7/00)

Micron Presentation at Special 42.3 Committee Meeting

Presented at JDEC

Programmable by pin stripping

Latency Technology Market
Cost Impact

(12/91) (Programmable Burst Length)

Mitsubishi Presentation at 42.3 Committee Meeting 60

Not Presented at JEDEC

Programmable in Read command

Latency Technology Market
Testimony at 5382

would be a cheaper alternative potentially. Jacob Trel
instead of having to test all possible CAS latency values, so it
fuse, you would only need to test one CAS latency value
design and therefore a cheaper design. After blooming the
eliminate the mode register. It would be potentially a smaller
It would be potentially a smaller design. You would

Cost impact

Cray presentation at 42.3 Committee Meeting 62 (5/92)

Presented at JDEC

Set by fuses

Latency Technology Market
Burst Length Technology Market

Cost Impact

- NEC Presentation at 42.3 Committee Meeting 76 (9/95)
- Presented at JDEC
- Fixed burst length
Burst Length Technology Market
cheaper to manufacture. Jacob Trial Testimony at 5407-408
make the part simpler to design and test and potentially
therefore the circuitry required to initialize it, which would

■ Well, again, you would get rid of the mode register and

Cost Impact

(12/91)

Mitsubishi Presentation at 42.3 Committee Meeting 60

■ Presented at JEDEC

■ Programmable in Read command

Burst Length Technology Market
words, they said this is easy. "Mean Trial Testimony at 4775
DRAM designers. The DRAM designers, I recall their
burst interrupt and it is fixed, and it's not a burden to the

- I mean, for DDR2, the DDR2 SDRAM standard, we do have
  Cost impact
  Proposal for DDR-2
  In SDRAM and DDR SDRAM standards and
  Burst interrupt

Burst Length Technology Market
benefit to single edge clocking. Macin Teti's testimony at
4779-4780

clocking doesn't have that issue at all. So, that's a huge
clocking conditions. It sounds simple, very complicated. Single edge
pulse, and managing that is very difficult across real world
is the length of the high pulse versus the length of the low
pulse that is high and a pulse that is low, and the duty cycle
called duty cycle. Duty cycle -- you know, a clock has a
calculated in that we don't have to pay attention to this concept
beneath. Well, a faster single edge clock has some enormous
Cost impact

VLSI Presentation at 42.3 Committee Meeting 78 (3/96)
Presented at JDEC
Double the clock frequency

Data Acceleration Technology Market
than just using an on-chip DLL alone. Jacob Trial Testimony itself, so you could potentially reach higher rates of speed
uncertainty than simply putting the DLL out on the DRAM
take less time. And it would cancel out more timing
take less time. And it would cancel out more timing.

Because it would not include a DLL and therefore cheaper,
that would be part of the DRAM. It would be a simpler design
because you don't have this PLL or rather, this DLL
because you don't have this PLL or rather, this DLL

The cost of the DRAM. You would reduce the testing costs of the
die size of the DRAM, which would reduce the manufacturing
dice size of the DRAM, which would reduce the manufacturing

"You would eliminate the on-chip DLL, which would reduce
the power consumption of the DRAM. It would reduce the
the power consumption of the DRAM. It would reduce the

Cost Impact

You would eliminate the on-chip DLL, which would reduce
the power consumption of the DRAM. It would reduce the
the power consumption of the DRAM. It would reduce the

Put the DLL on the memory controller

Clock Synchronization Technology Market

Samsung Presentation at 42.3 Committee Meeting 78 (3/96)

Presented at JDEC
would be trading one for the other. Jacob Trial Testimony at
onto a special DLL chip that goes onto the module, so you
the design time. You then move that design complexity
reducing its power consumption, reducing its cost, reducing

"You eliminate the on-chip DLL from the DRAM, thereby

Cost Impact

QBM DIMM

PLL on DIMM in Registered DIMMs and in Kerton

PLL/DLL on module

Clock Sych Technology Market
Jacob Trial Testimony at 5452

achieve higher data rates using it. And burn less power

potentially more skew than a DLL so you could potentially

It’s simpler to design than a DLL and it would cancel out

Cost Impact

Synclink Presentation at 42.3 Committee Meeting 75 (5/95)

Presented at JDEC

Vernier

Clock Synch Technology Market
Jacob Trial Testimony at 5457 Ford.

For the design would be smaller, cheaper to manufacture, and so your design simpler. It would consume less power. The chip DILL?

- A. Well, you would eliminate your DLL, which would make the Cost impact?

- SCSI Presentation at 42.3 Interim Committee Meeting (7/97)

- Presented at JEDEC

- No DLL at all

Clock Synchron Technology Market
Testimony at 5395-96

Performance and cheaper implementation. Jacob Tral

same speeds. So asynchronous potentially had better

smaller die size than SDRAM and had better performance at the
time had a smaller die size like burst EDO at the time. This was a technology

existed at the time. This was a technology that the engineers of

ITW had been a simpler transition because the technology

Cost Impact

 NEC Presentation at 42.3 Committee Meeting (3/95)

 Often presented at JDEC

Length in SDRAM

 Alternative to both programmable CAS latency and burst

Asynchronous - Burst EDO
Conduct Is Exclusory

Reasons Why Rambus’s Challenges

Enforceability of patented intellectual property

Entailed a conscious choice to jeopardize the

Technologies

Excluded alternative commercially viable DRAM

Information

Concealing (or misrepresenting) material

Distorted JEDEC’s standard setting process by
Without RANO letter, JEDEC could not include IP in standard.

- Not issuing RANO letter could have helped RDRAM succeed.
- Rambus wanted RDRAM to succeed rates.
- Rambus wanted flexibility to charge different royalty rates.
- Rambus wanted a business model.
- Rambus documents state RANO not consistent with

**NO RANO Letter**

If Rambus had disclosed IP to JEDEC:
competition absent expected benefits from excluding
like predatory pricing, this conduct is irrational

implication is that Rambus expected compensating
incurred risk of having patients found unenforceable
By not disclosing IP ex ante, Rambus knowingly

Rambus’s Costly Investment Exclusory Conduct: